CHAPTER 14

Linear Power Supplies

Learning Objectives

After completing this chapter, you will learn the following:

- Constituents of a linear power supply and the role of different building blocks.
- Designing mains transformer.
- Different types of rectifier circuits and their characteristic features.
- Different types of filter circuits and their characteristic features.
- Different types of linear regulator circuits.
- Emitter–follower regulator.
- Series-pass element regulators.
- Shunt regulators.
- Protection circuits.
- IC voltage regulators including general-purpose, fixed output and adjustable output regulators.

Every electronics system, be it an entertainment gadget or a test and measurement equipment, requires one or more DC voltages for its operation. Most of the time it is essential and almost always desirable that these DC voltages are nicely filtered and well regulated. Power supply does the job of providing required DC voltages from available AC mains in the case of mains operated systems and DC input in the case of battery operated systems. Power supplies are often classified as linear power supplies or switched mode power supplies depending upon the nature of regulation circuit. While in the present chapter, the focus is on linear power supplies; switched mode power supplies are discussed in the next chapter.

14.1 Constituents of a Linear Power Supply

A linear power supply essentially comprises a *mains transformer*, a *rectifier circuit*, a *filter circuit* and a *regulation circuit* (Figure 14.1). The transformer provides voltage transformation and produces across its secondary winding(s) AC voltage(s) required for producing desired DC voltages. It also provides electrical isolation between the input power supply, that is, AC mains and the DC output. Step-down transformers required for generating common DC voltages and load current ratings are commercially available. Step-up transformers for generating higher output voltages could be custom designed. Different steps involved in the design of a mains transformer for given primary and secondary voltages and secondary current specifications are outlined in Section 14.2.

The rectifier circuit changes the AC voltage appearing across transformer secondary to DC or more precisely a unidirectional output. Commonly used rectifier circuits include the half-wave rectifier, conventional full-wave rectifier requiring a tapped secondary winding and the bridge rectifier.

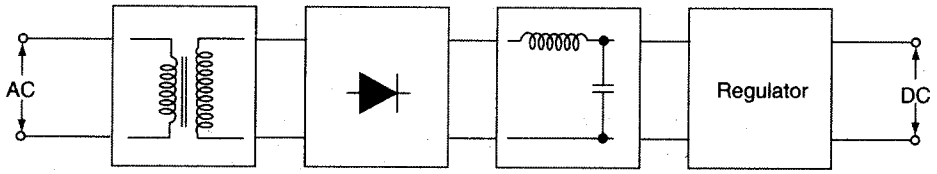


Figure 14.1 | Constituents of a linear power supply.

The rectifier voltage always has some AC content known as ripple. The filter circuit smoothens the ripple of the rectifier voltage. The regulator circuit is a type of feedback circuit that ensures that the output DC voltage does not change from its nominal value due to change in line voltage or load current.

In a linearly regulated power supply, the active device used in the regulator, usually a bipolar transistor, is operated anywhere between cut-off and saturation. Commonly used regulator circuit configurations include emitter–follower regulator, series-pass regulator and shunt regulator. Emitter–follower and series-pass regulators are, in fact, now available in IC packages in both fixed output voltage as well as variable output voltage varieties. These are popularly known as *three terminal regulators* and are discussed in Section 14.6.

All power supplies have in-built protection circuits. Common protection features include current limit, short-circuit protection, thermal shutdown and crowbaring. These are also discussed in the chapter.

14.2 Designing Mains Transformer

As outlined earlier, mains transformers for various primary voltages, secondary voltages and a range of secondary current ratings are commercially available to meet most of power supply designers' requirements. In the case of any special requirements, mains transformers can be custom designed by following the under-mentioned steps.

1. The first step is to ensure that the transformer does not saturate at the desired load current or output power requirement. Choosing the transformer core with appropriate cross-section does this. The optimum core cross-section (A_C) is determined with sufficient accuracy using the following equation:

$$A_C = \frac{\sqrt{P}}{5.6} \tag{14.1}$$

where P is the power required to be delivered by the transformer in Watts; A_C the core cross-section in square inches.

2. The ratio of stack thickness (t) to the width of the center limb (W) should be in the range of 1.1 to 1.5 (Figure 14.2).
3. The turns per volt for different windings can be computed as

$$\text{Turns per volt} = \frac{10^8}{4.44 \times f \times A_C \times B} \tag{14.2}$$

where f is the frequency in Hz; B the flux density in lines per square inch (for STALLOY and other similar core materials used for winding power transformers, B may be taken as 50,000 lines per square inch); A_C the core cross-section in square inch. In Eq. (14.2), if core cross-section (A_C) were substituted in cm^2, then the flux density (B) should be substituted in Gauss.

4. Having computed turns per volt, primary and secondary number of turns can be computed from known values of primary and secondary voltages.

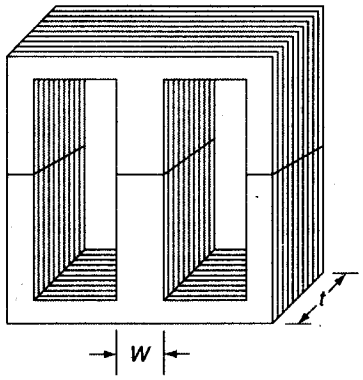


Figure 14.2 | Designing mains transformer.

5. Primary current is computed as

$$\text{Primary current} = \frac{P}{\text{Efficiency} \times \text{Primary voltage}} \tag{14.3}$$

Efficiency may be taken as 85–90%.

6. Secondary current is computed as

$$\text{Secondary current} = \frac{\text{Primary current}}{n} \tag{14.4}$$

where n is the ratio of secondary turns (N_S) to primary turns (N_P).

Primary and secondary wire sizes can be determined from known values of primary and secondary currents. Standard wire gauge table can be referred to know the wire gauge number. For power transformers, it is reasonably safe to assume current density figure of 2000 A/in.^{2}. The current handling capability of wires of different sizes in standard wire gauge table is usually given with the assumption of current density figure of 1000 A/in.^{2}.

EXAMPLE 14.1

Design a power transformer with a multi-output secondary and the following input/output specifications.

(a) Primary voltage: 220 V, 50 Hz.

(b) Secondary voltage: (a) 12–0–12 V at 100 mA and (b) 5 V at 1 A.

Assume B = 60,000 lines per square inch for the chosen core material and an efficiency of 90%.

Solution

1. Power to be delivered by transformer secondary = $12 \times 0.1 + 5 \times 1 = 6.2$ W.
2. Core cross-section, $A_C = \sqrt{P}/5.6$, where P is the power to be delivered by transformer secondary. Therefore, $A_C = \sqrt{6.2}/5.6 = 0.444$ in.^{2}.
3. Turns per volt = $10^8/[4.44 \times f \times A_C \times B] = 10^8/[4.44 \times 50 \times 0.444 \times 60{,}000] = 16.9$.
4. Therefore, number of primary turns = $16.9 \times 220 = 3718$.
5. The number of secondary turns for one half of (12–0–12) V center-tapped winding = $16.9 \times 12 = 203$.

6. The number of secondary turns for 5 V winding = 16.9 × 5 = 85.
7. Primary current = 6.2/(0.9 × 220) = 0.03 A.
8. Secondary current in (12–0–12) V winding = 0.1 A.
9. Secondary current in 5 V winding = 1 A.
10. The wire sizes for the primary winding, (12–0–12) V secondary winding and 5 V secondary winding, respectively, are 40 SWG, 35 SWG and 23 SWG assuming a current density of 2000 A/in.^{2}.

14.3 Rectifier Circuits

As outlined earlier, the job of rectifier circuit is to convert the AC voltage appearing across the transformer secondary into a unidirectional voltage. There are three basic rectifier circuit configurations. These include (a) half-wave rectifier, (b) conventional two-diode full-wave rectifier that requires a center-tapped secondary winding and (c) bridge rectifier. Rectifier circuits are characterized by several parameters, which include *ripple frequency, ripple factor, ratio of rectification, transformer utilization factor* and the required *peak inverse voltage* of the rectifier diodes in the circuit. These parameters are briefly discussed in the following subsections. This is then followed up by discussion on different types of rectifier circuits with particular reference to their comparison on the basis of these parameters.

Characteristic Parameters

Performance of a rectifier circuit is often judged on the basis of the parameters outlined in the previous paragraph. These parameters are briefly covered in the following paragraphs.

Ripple Frequency

Ripple frequency is the frequency of the unidirectional periodic voltage waveform present at the output of the rectifier circuit. In the case of half-wave rectifier, as we will see when we discuss different rectifier circuits, it is f, where f is the frequency of AC signal present at the input of rectifier circuit. In the case of full-wave rectifiers, conventional and bridge, it is $2f$. The significance of ripple frequency lies in its direct relationship with ripple factor. Higher ripple frequency means lower ripple factor and less stringent filtering requirement.

Ripple Factor

Ripple factor is ratio of root mean square (RMS) amplitude of AC component (ripple) to the DC component in the rectified waveform. Ripple factor tells how close the rectified waveform is to the true DC. It can be computed as ratio of RMS value of AC component of the rectified voltage signal to the DC component of the rectified voltage signal. It can also be computed from the ratio of RMS value of AC component of rectified current signal to the DC component of the rectified current signal. That is, ripple factor (r) is given by

$$r = \frac{V_r(\text{RMS})}{V_{DC}} = \frac{I_r(\text{RMS})}{I_{DC}}$$

where V_r (RMS) is the RMS value of ripple voltage; V_{DC} the DC value of rectified voltage; I_r (RMS) the RMS value of ripple current; I_{DC} the DC value of rectified current. Also,

$$V_r(\text{RMS}) = \sqrt{V_{\text{RMS}}^2 - V_{DC}^2}$$

where V_{RMS} is the RMS value of the rectified voltage. I_r (RMS) is given by

$$I_r(\text{RMS}) = \sqrt{I_{RMS}^2 - I_{DC}^2}$$

where I_{RMS} is the RMS value of the rectified current. This gives ripple factor as

$$r = \sqrt{\frac{V_{RMS}^2 - V_{DC}^2}{V_{DC}^2}} = \sqrt{\frac{I_{RMS}^2 - I_{DC}^2}{I_{DC}^2}}$$

$$r = \sqrt{\left(\frac{V_{RMS}}{V_{DC}}\right)^2 - 1} = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1} \tag{14.5}$$

Ratio of Rectification

Ratio of rectification is the ratio of DC power delivered to the load to the AC power input from transformer secondary. Like ripple factor, it also determines the effectiveness of a rectifier circuit in converting AC into DC. DC power delivered to the load resistance (R_L) = $I_{DC}^2 \times R_L$. AC power input from transformer secondary = $I_{RMS}^2 \times (R_f + R_L)$. Here R_f is the resistance offered by forward-biased rectifier diode. Since R_f is much smaller than R_L, AC power available from transformer secondary $\cong I_{RMS}^2 \times R_L$. This gives,

$$\text{Ratio of rectification} = \frac{I_{DC}^2}{I_{RMS}^2} = \left(\frac{I_{DC}}{I_{RMS}}\right)^2 \tag{14.6}$$

From Eqs. (14.5) and (14.6) we can see that ratio of rectification and ripple factor are interrelated. One can be expressed in the form of the other and vice versa. The interrelationship is determined in Example 14.2.

Transformer Utilization Factor

Transformer utilization factor (*TUF*) is defined as the ratio of DC power delivered to the load to the AC power rating of the transformer secondary:

$$\text{TUF} = \frac{\text{DC power delivered to the load}}{\text{AC power rating of transformer secondary}}$$

It may be mentioned here that rating of the transformer in a power supply is governed by the intended DC power to be delivered to the load and the type of rectifier circuit. TUF parameter should not be confused with the ratio of rectification. Rating of transformer secondary is different from the actual AC power delivered by it. AC power rating of transformer secondary is the product of RMS value of voltage across secondary and RMS value of current flowing through secondary. The transformer utilization factor tells us about the maximum DC power that can be delivered to the load for a given transformer rating. A lower TUF implies lower DC power delivered to load for a given power rating of the transformer. We will see in the following paragraphs that TUF values for half-wave and full-wave rectifiers, respectively, are 0.287 and 0.574. This implies that a 1 kVA transformer can at the most deliver a DC power of 287 W to a resistive load when used with a half-wave rectifier. The same for a full-wave rectifier is 574 W.

Peak Inverse Voltage

Peak inverse voltage is the maximum reverse voltage appearing across the diodes used in the rectifier circuit. It is important as it decides the PIV rating of the diode to be used in the rectifier circuit. It is yet another parameter that can be used to compare merits/demerits of different rectifier circuits. It is V_m, $2V_m$ and V_m in the case of half-wave, conventional two-diode full-wave and bridge rectifier circuits, respectively.

Half-Wave Rectifier

Figure 14.3 shows the half-wave rectifier circuit for positive output voltage along with input and output waveforms. Figure 14.4 shows the same for negative output voltage. In the case of positive output rectifier circuit of Figure 14.3, diode D_1 is forward-biased during positive half cycles and reverse-biased during negative half cycles of the input. In the case of negative output rectifier circuit of Figure 14.4, diode D_1 is forward-biased during negative half cycles and reverse-biased during positive half cycles of the input. This explains the output waveforms in the two cases.

Ripple factor in the case of half-wave rectifier circuit can be computed from Eq. (14.5) as

$$r = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1}$$

In the case of a half-wave rectified waveform,

$$I_{RMS} = \frac{I_m}{2} \quad \text{and} \quad I_{DC} = \frac{I_m}{\pi}$$

where I_m is the peak value of the current waveform across the secondary. This gives

$$r = \sqrt{\left(\frac{I_m/2}{I_m/\pi}\right)^2 - 1} = \sqrt{(\pi^2/4) - 1} = 1.21$$

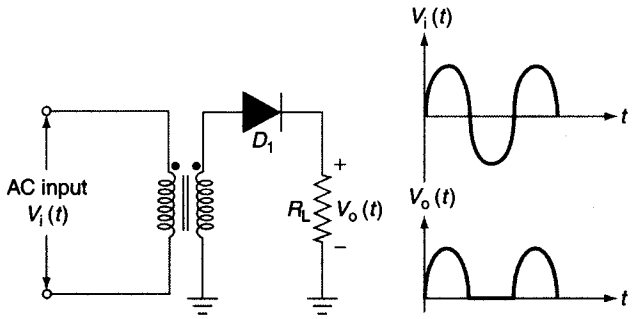


Figure 14.3 | Half-wave rectifier circuit for positive output voltage.

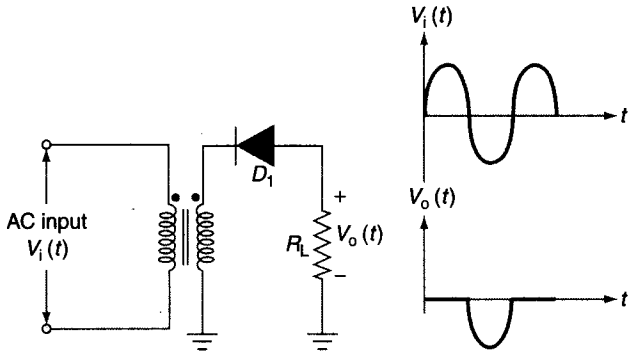


Figure 14.4 | Half-wave rectifier for negative output voltage.

Ratio of rectification can be computed from Eq. (14.6) as

$$\text{Ratio of rectification} = \left(\frac{I_{DC}}{I_{RMS}}\right)^2 = \left(\frac{I_m/\pi}{I_m/2}\right)^2 = \frac{4}{\pi^2} = 0.406$$

Transformer utilization factor can be computed as follows:

$$\text{DC power delivered to load} = \left(\frac{I_m}{\pi}\right)^2 \times R_L$$

$$\text{AC power rating of transformer secondary} = \frac{V_m}{\sqrt{2}} \times \frac{I_m}{2} = \frac{V_m \times I_m}{2\sqrt{2}}$$

Also, ignoring the forward-biased diode's resistance, $V_m = I_m \times R_L$. This gives

$$\text{AC power rating of transformer secondary} = \frac{V_m \times I_m}{2\sqrt{2}} = \frac{I_m^2 \times R_L}{2\sqrt{2}}$$

Therefore,

$$\text{Transformer utilization factor} = \frac{(I_m/\pi)^2 \times R_L}{(I_m^2 \times R_L)/2\sqrt{2}} = \frac{2\sqrt{2}}{\pi^2} = 0.287$$

Full-Wave Rectifier

Figure 14.5 shows the full-wave rectifier circuit for positive output voltage along with input and output waveforms. Figure 14.6 shows the same for negative output voltage. In the case of positive output rectifier circuit of Figure 14.5, diode D_1 is forward-biased and diode D_2 is reverse-biased during positive half cycles of the input. During negative half cycles, diode D_2 is forward-biased and diode D_1 is reverse-biased. In both half cycles, current through load resistance R_L flows in the same direction as shown. In the case of negative output rectifier circuit of Figure 14.6, diode D_2 is forward-biased and diode D_1 is reverse-biased during positive half cycles of the input. During negative half cycles, diode D_1 is forward-biased and diode D_2 is reverse-biased. In both half cycles, current through load resistance R_L flows in the same direction, which is opposite to the direction of flow of current in the case of positive output circuit. This explains the output waveforms in the two cases.

Ripple factor in the case of full-wave rectifier circuit can be computed from Eq. (14.5) as

$$r = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1}$$

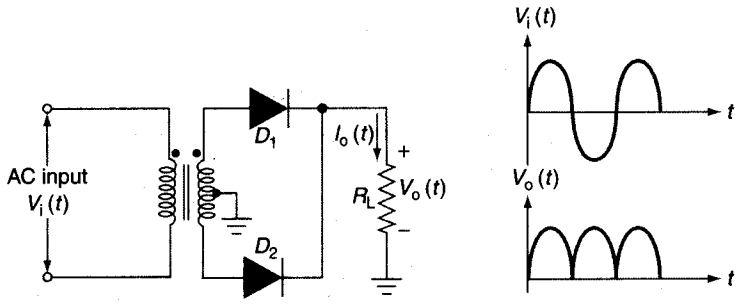


Figure 14.5 Full-wave rectifier circuit for positive output voltage.

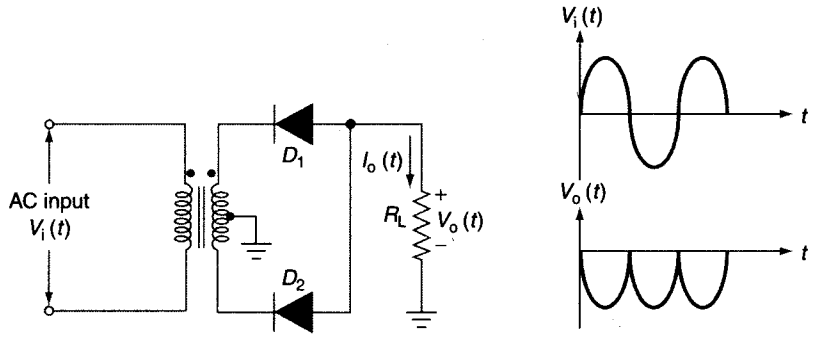


Figure 14.6 | Full-wave rectifier for negative output voltage.

In the case of a full-wave rectified waveform,

$$I_{RMS} = \frac{I_m}{\sqrt{2}} \quad \text{and} \quad I_{DC} = \frac{2I_m}{\pi}$$

where I_m is the peak value of the current waveform, we have

$$r = \sqrt{\left(\frac{I_m/\sqrt{2}}{2I_m/\pi}\right)^2 - 1} = \sqrt{(\pi^2/8) - 1} = 0.482$$

Ratio of rectification can be computed from Eq. (14.6) as

$$\text{Ratio of rectification} = \left(\frac{I_{DC}}{I_{RMS}}\right)^2 = \left(\frac{2I_m/\pi}{I_m/\sqrt{2}}\right)^2 = \frac{8}{\pi^2} = 0.812$$

Transformer utilization factor can be computed as follows:

$$\text{DC power delivered to load} = \left(\frac{2I_m}{\pi}\right)^2 \times R_L$$

$$\text{AC power rating of transformer secondary} = 2 \times \left(\frac{V_m}{\sqrt{2}} \times \frac{I_m}{2}\right) = \frac{V_m \times I_m}{\sqrt{2}}$$

Also, ignoring the forward-biased diode's resistance, we get $V_m = I_m \times R_L$. This gives

$$\text{AC power rating of transformer secondary} = \frac{V_m \times I_m}{\sqrt{2}} = \frac{I_m^2 \times R_L}{\sqrt{2}}$$

Therefore,

$$\text{Transformer utilization factor} = \frac{(2I_m/\pi)^2 \times R_L}{(I_m^2 \times R_L)/\sqrt{2}} = \frac{4\sqrt{2}}{\pi^2} = 0.574$$

Bridge Rectifier

Figure 14.7 shows the bridge rectifier circuit for positive output voltage along with input and output waveforms. Figure 14.8 shows the same for negative output voltage. In the case of positive output rectifier circuit of Figure 14.7, diodes D_1 and D_3 are forward-biased and diodes D_2 and D_4 are reverse-biased during positive half cycles of the input. During negative half cycles, diode D_2 and D_4 are forward-biased and diodes D_1 and D_3 are reverse-biased. In both half cycles, current through load resistance R_L flows in the same direction as shown. In the case of negative output rectifier circuit of Figure 14.8, diodes D_2 and D_4 are forward-biased and diodes D_1 and D_3 are reverse-biased during positive half cycles of the input. During negative half cycles, diodes D_1 and D_3 are forward-biased and diodes D_2 and D_4 are reverse-biased. In both half cycles, current through load resistance R_L flows in the same direction, which is opposite to the direction of flow of current in the case of positive output circuit. This explains the output waveforms in the two cases.

Ripple factor and ratio of rectification parameters in the case of bridge rectifier are the same as those computed in the case of two-diode full-wave rectifier. That is, ripple factor = 0.482 and ratio of rectification = 0.812. Transformer utilization factor can be computed as follows:

$$\text{DC power delivered to load} = \left(\frac{2I_m}{\pi}\right)^2 \times R_L$$

$$\text{AC power rating of transformer secondary} = \frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}} = \frac{V_m \times I_m}{2}$$

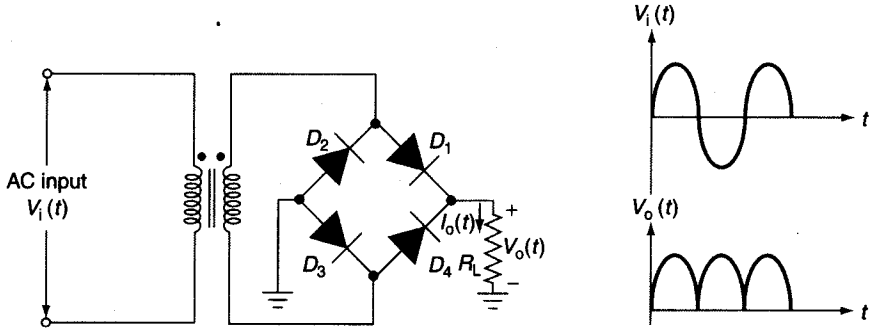


Figure 14.7 | Bridge rectifier for positive output voltage.

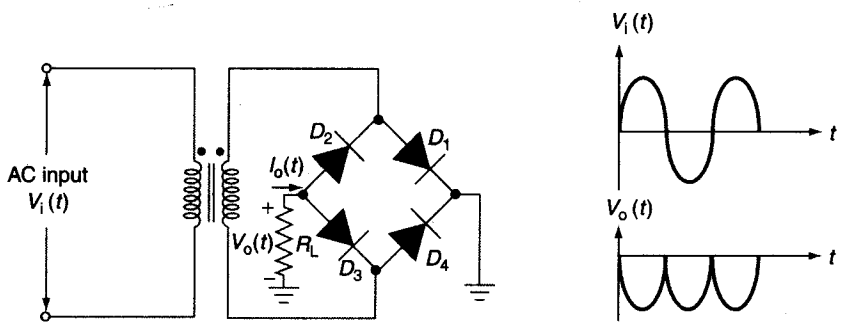


Figure 14.8 | Bridge rectifier for negative output voltage.

Table 14.1 | Comparison of rectifier circuits

Parameter	Half wave	Full wave	Bridge
Secondary voltage Line-to-line (RMS)	$\frac{V_m}{\sqrt{2}}$	$\sqrt{2} \times V_m$	$\sqrt{2} \times V_m$
Number of diodes	1	2	4
Peak inverse voltage	V_m	$\sqrt{2} \times V_m$	V_m
No load DC output	$\frac{V_m}{\pi}$	$\frac{2V_m}{\pi}$	$\frac{2V_m}{\pi}$
Ripple frequency	f	$2f$	$2f$
Ripple factor	1.21	0.482	0.482
Ratio of rectification	0.406	0.812	0.812
TUF	0.287	0.574	0.812

Also, ignoring the forward-biased diode's resistance, we get $V_m = I_m \times R_L$. This gives

$$\text{AC power rating of transformer secondary} = \frac{V_m \times I_m}{2} = \frac{I_m^2 \times R_L}{2}$$

Therefore,

$$\text{Transformer utilization factor} = \frac{(2I_m/\pi)^2 \times R_L}{(I_m^2 \times R_L)/2} = \frac{8}{\pi^2} = 0.812$$

Table 14.1 gives a comparison of different rectifier circuits.

EXAMPLE 14.2

Ripple factor and ratio of rectification are related to each other. Derive an expression to show how ratio of rectification can be expressed in terms of ripple factor.

Solution

1. Ripple factor, r, is given by Eq. (14.5) as

$$r = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1}$$

2. This gives

$$\left(\frac{I_{RMS}}{I_{DC}}\right)^2 = 1 + r^2 \quad \text{or} \quad \left(\frac{I_{DC}}{I_{RMS}}\right)^2 = \frac{1}{1+r^2}$$

3. Ratio of rectification is given by Eq. (14.6) as

$$\text{Ratio of rectification} = \left(\frac{I_{DC}}{I_{RMS}}\right)^2 = \frac{1}{1+r^2}$$

EXAMPLE 14.3

Determine the transformer rating if it were to deliver a DC power of 500 W to a resistive load using (a) half-wave rectifier, (b) conventional two-diode full-wave rectifier and (c) bridge rectifier.

Solution

(a) In the case of half-wave rectifier,

Transformer utilization factor = 0.287 = DC power delivered to load/transformer rating

Therefore, transformer rating = DC power delivered to load/0.287 = 500/0.287 = 1742 W.

(b) In the case of conventional two-diode full-wave rectifier,

Transformer utilization factor = 0.574 = DC power delivered to load/transformer rating

Therefore, transformer rating = DC power delivered to load/0.574= 500/0.574 = 871 W.

(c) In the case of bridge rectifier,

Transformer utilization factor = 0.812 = DC power delivered to load/transformer rating

Therefore, transformer rating = DC power delivered to load/0.812 = 500/0.812 = 616 W.

EXAMPLE 14.4

A 220 V, 50 Hz AC is applied to the primary of 5:1 step-up transformer with a tapped secondary winding. The transformer along with a two-diode full-wave rectifier feeds a resistive load of 1000 Ω. Determine (a) DC power delivered to the load, (b) power rating of the transformer secondary, (c) PIV across each diode and (d) ripple frequency and ripple factor.

Solution

(a) Peak value of primary voltage = $220 \times \sqrt{2} = 311$ V.

Peak value of secondary voltage = $311 \times 5 = 1555$ V.

Peak value of secondary current = 1555/1000 = 1.555 A.

DC power delivered to the load = $(2 \times 1.555/\pi)^2 \times 1000 = 981$ W.

(b) In the case of two-diode full-wave rectifier, transformer utilization factor = 0.574. Therefore, power rating of transformer secondary = 981/0.574 = 1709 W.

(c) PIV across each diode = $2 \times 1555 = 3.11$ kV.

(d) Ripple frequency = $2 \times f = 2 \times 50 = 100$ Hz.

$$\text{Ripple factor} = \sqrt{(I_{RMS} / I_{DC})^2 - 1}$$

$$I_{RMS} = 1.555/\sqrt{2} = 1.1 \text{ A}$$

$$I_{DC} = 2 \times 1.555/\pi = 0.99 \text{ A}$$

Therefore, ripple factor = $\sqrt{(1.1/0.99)^2 - 1} = 0.484$.

14.4 Filters

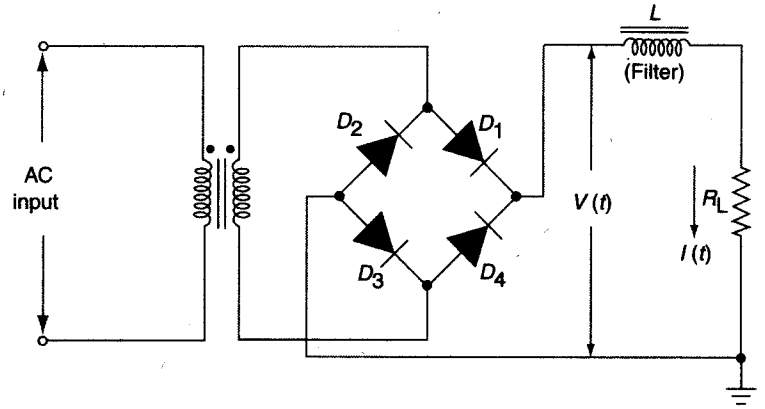
The filter in a power supply helps in reducing the ripple content (the amplitude of AC component), which in the rectified waveform is so large that the waveform can hardly be called a DC. Inductors, capacitors and inductor–capacitor combinations are used for the purpose of filtering. Each one of these types of filters is described in the following sub-sections.

Inductor Filter

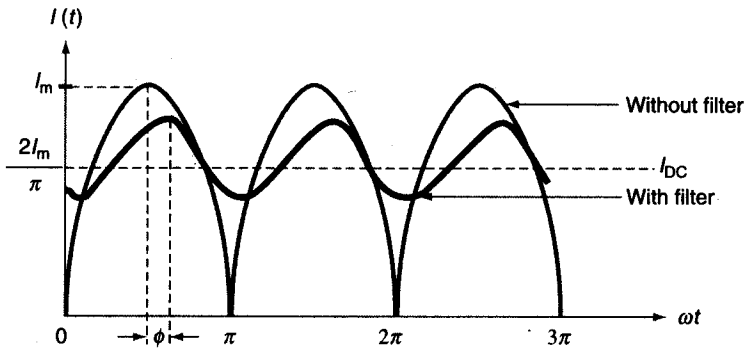
The fact that an inductor offers high reactance to AC components is the basis of filtering provided by inductors. Figure 14.9(a) shows the full-wave rectifier circuit with inductor filter. The load current waveforms with and without filter are shown in Figure 14.9(b). The ripple factor (r) can be determined to be equal to $R_L/[3\sqrt{2}(\omega L)]$, which equals $R_L/1333L$ for power line frequency of 50 Hz and $R_L/1600L$ for power line frequency of 60 Hz. Here L is in henries and R_L is in ohms. Equation for ripple factor is derived as follows.

The Fourier series expansion of a full-wave rectified voltage waveform is given by

$$V(t) = \frac{2V_m}{\pi} - \frac{4V_m}{\pi}\left[\left(\frac{\cos 2\omega t}{3}\right) + \left(\frac{\cos 4\omega t}{15}\right) + \left(\frac{\cos 6\omega t}{35}\right) + \cdots\right] \tag{14.7}$$



(a)



(b)

Figure 14.9 | Inductor (or choke) filter.

Neglecting higher order terms beyond second harmonic, Eq. (14.7) reduces to

$$V(t) = \frac{2V_m}{\pi} - \left(\frac{4V_m}{3\pi}\right)\cos 2\omega t \tag{14.8}$$

In Eq. (14.8), the first term represents the DC component and the second term represents the AC component.

Since the AC component of current will lag behind the voltage by an angle (ϕ) given by $\tan^{-1}(2\omega L/R_L)$, the expression for resulting current can be written as follows:

$$I(t) = \left(\frac{2V_m}{\pi R_L}\right) - \left(\frac{4V_m}{3\pi}\right) \times \left(\frac{1}{\sqrt{R_L^2 + 4\omega^2 L^2}}\right) \times \cos(2\omega t - \phi) \tag{14.9}$$

Ripple factor is nothing but the ratio of RMS value of the AC component to that of the DC component. It can be computed from Eq. (14.9) as it contains both the DC component and the peak value of the AC component. It is given by

$$r = \left(\frac{4V_m}{3\pi\sqrt{2}}\right) \times \left(\frac{1}{\sqrt{R_L^2 + 4\omega^2 L^2}}\right) \times \frac{\pi R_L}{2V_m} = \frac{\sqrt{2}}{3\sqrt{1 + (4\omega^2 L^2/R_L^2)}} \tag{14.10}$$

For $4\omega^2 L^2/R_L^2$ much greater than 1, the expression for ripple factor (r) reduces to

$$r = \frac{R_L}{3\sqrt{2}(\omega L)} \tag{14.11}$$

As is clear from the above expression, the ripple factor is directly proportional to load resistance (R_L). That is, the ripple content increases with increase in load resistance. In other words, choke filter is not effective for light loads (or high values of load resistance) and is preferably used for relatively higher load currents. In the limit when load resistance tends to infinity (for no load condition), from the exact expression of ripple factor as given in Eq. (14.10), we get $r = \sqrt{2}/3 = 0.471$. This value is very close to the value derived earlier in the case of full-wave rectifier without filter. The slight difference can be attributed to omission of higher order terms in Eq. (14.7). It therefore implies that presence of inductor filter is as good as not there in the case of load resistance tending to become infinity. In other words, an inductor filter becomes less and less effective with increase in value of load resistance.

It may also be noted that with inductive filtering, the load current never drops to zero. If the value of inductance is suitably chosen, the flow of current through the diodes and the secondary of the transformer are much more even than it would have been without the filter. This leads to ratio of rectification of almost unity due to RMS and DC values of the filtered current waveform to be almost the same and an improved transformer utilization factor.

Capacitor Filter

The filtering action of a capacitor connected across the output of the rectifier comes from the fact that it offers a low reactance to AC components. Figure 14.10(a) shows a capacitor filter connected across the output of a full-wave rectifier. The AC components are bypassed to ground through the capacitor and only the DC is allowed to go through to the load. The capacitor charges to the peak value of the voltage waveform during the first cycle and as the voltage in the rectified waveform is on the decrease, the capacitor voltage is not able to follow the change as it can discharge only at a rate determined by (CR_L) time constant. In the case of light loads (or high values of load resistance), the capacitor would discharge only a little before the voltage in the rectified waveform exceeds the capacitor voltage thus charging it again to the peak value [Figure 14.10(b)]. The ripple content is inversely proportional to C and R_L.

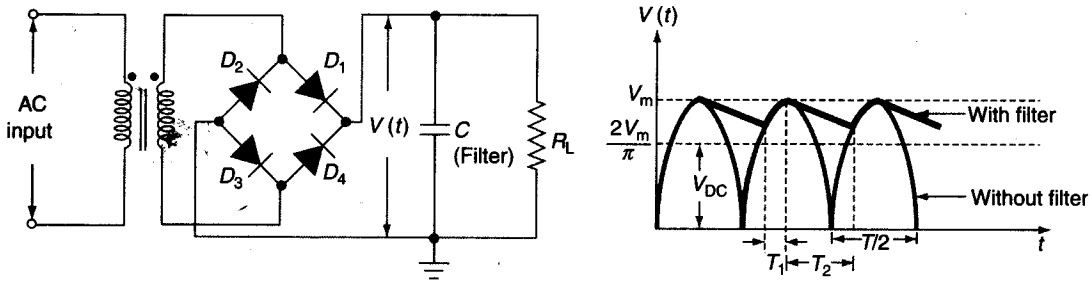


Figure 14.10 | Capacitor filter.

Ripple can be reduced by increasing C for a given of R_L. For heavy loads when R_L is small, even a large capacitance value may not be able to provide ripple within acceptable limits. Ripple factor can be computed as follows.

Referring to the waveform of Figure 14.10(b), to a reasonable approximation, the ripple waveform can be considered to be a triangular one. The charge acquired by the filter capacitor during the time it is charging [T_1 in Figure 14.10(b)] equals the charge lost by it during the time it is discharging through load resistance R_L [T_2 in Figure 14.10(b)].

$$\text{Charge acquired} = V_r\,(\text{peak-to-peak}) \times C \tag{14.12}$$

$$\text{Charge lost} = I_{DC} \times T_2 \tag{14.13}$$

Equating the two, we get

$$V_r\,(\text{peak-to-peak}) \times C = I_{DC} \times T_2 \tag{14.14}$$

In the case of a large CR_L, time period T_2 equals $T/2$ where T is the time period of the AC input. This gives

$$V_r\,(\text{peak-to-peak}) \times C = \frac{I_{DC} \times T}{2} \tag{14.15}$$

$$V_r\,(\text{peak-to-peak}) = \frac{I_{DC} \times T}{2C} = \frac{I_{DC}}{2fC} \tag{14.16}$$

Assuming a triangular ripple waveform as outlined earlier, we get

$$\text{RMS value of the waveform} = \frac{V_r\,(\text{peak})}{\sqrt{3}}$$

Therefore,

$$V_r\,(\text{RMS}) = \frac{V_r\,(\text{peak-to-peak})}{2\sqrt{3}} = \frac{I_{DC} \times T}{4\sqrt{3}C} = \frac{I_{DC}}{4\sqrt{3}fC} \tag{14.17}$$

Also, $I_{DC} = V_{DC}/R_L$. Therefore,

$$V_r\,(\text{RMS}) = \frac{V_{DC}}{4\sqrt{3}fCR_L} \tag{14.18}$$

$$\text{Ripple factor, } r = \frac{V_r\,(\text{RMS})}{V_{DC}} = \frac{1}{4\sqrt{3}fCR_L} \tag{14.19}$$

Ripple factor (r) equals $2887/CR_L$ for power line frequency of 50 Hz and $2406/CR_L$ for a power line frequency of 60 Hz. Here C is in microfarads and R_L is in ohms. It may be mentioned here that the above expression for ripple factor holds good in the case of an ideal capacitor with a zero equivalent series resistance (ESR). In the case of practical capacitors, the ESR is easily of the order of several ohms or even a few tens of ohms for the large values of capacitance encountered in filter capacitors. In such cases, the ripple factor deteriorates from the value computed from Eq. (14.19). The ESR should also be considered while computing the repetitive peak current during the charging process and also the surge current that would flow when the power is initially is switched on and the filter capacitor is fully discharged.

LC Filter

We have seen that while an inductance filter is effective only at heavy load currents, a capacitor filter provides adequate filtering only for light loads. The performance of inductor and capacitor filters deteriorates fast as the load resistance is increased in the case of former or decreased in the case of the latter. Apparently, an appropriate combination of L and C could give us a filter that would provide adequate filtering over a wide range of load resistance R_L values.

Figure 14.11 shows an LC filter connected across the output of a full-wave rectifier. If the value of inductance (L) in the LC filter is small, the filter will predominantly be a capacitor filter and the capacitor will repetitively charge to the peak value and cut off the diodes. The current in this case is in the form of short pulses only. An increase in the value of inductance allows the current to flow for longer periods. If the inductance is further increased, we reach a stage where one diode or the other is always conducting with the result that the current and voltage to the input of LC filter are full-wave rectified waveforms. This is known as the critical value of inductance (L_C). If the inductance (L) is equal to or more than the critical inductance, the voltage applied to the filter can be approximated by Eq. (14.20).

$$V(t) = \frac{2V_m}{\pi} - \left(\frac{4V_m}{3\pi}\right)\cos 2\omega t \tag{14.20}$$

The ripple factor in the case of LC filter can now be computed as follows. For a properly designed LC filter, $X_C << R_L$ and $X_L >> X_C$ at a radian frequency of 2ω. X_L therefore primarily determines the AC component of ripple. Therefore,

$$I_r(\text{RMS}) = \frac{4V_m}{3\pi\sqrt{2}X_L} = \frac{\sqrt{2}}{3} \times \frac{V_{DC}}{X_L} \quad \text{as} \quad V_{DC} = 2V_m/\pi \tag{14.21}$$

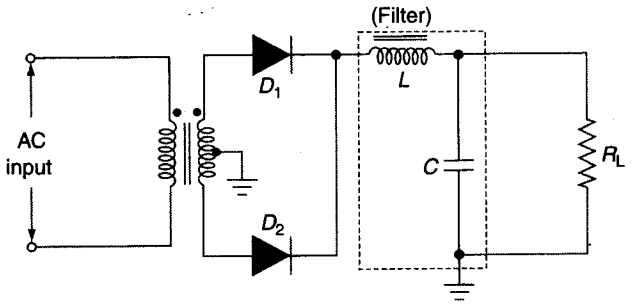


Figure 14.11 | LC filter.

Also,

$$V_r(\text{RMS}) = I_r(\text{RMS}) \times X_C = \left(\frac{\sqrt{2}}{3}\right) \times V_{DC} \times \left(\frac{X_C}{X_L}\right) = \left(\frac{\sqrt{2}X_C}{3X_L}\right) \times V_{DC} \tag{14.22}$$

$$\text{Ripple factor, } r = \frac{\sqrt{2}X_C}{3X_L} = \left(\frac{\sqrt{2}}{3}\right) \times \left(\frac{1}{4\omega^2 LC}\right) = \left(\frac{\sqrt{2}}{12\omega^2}\right) \times \left(\frac{1}{LC}\right) \tag{14.23}$$

Remember that the full-wave rectified waveform input to the filter has a radian frequency of 2ω.

The above expression proves that the ripple factor in a choke input LC filter is independent of R_L. Equation (14.23) reduces to $1.2/LC$ for power line frequency of 50 Hz and $0.83/LC$ for a power line frequency of 60 Hz. In this expression, L is in henries and C is in microfarads.

The chosen value of inductance should be greater than or equal to the critical inductance. The value of critical inductance is such that the DC value of current is equal to or greater than the negative peak of the AC component to ensure a continuous flow of current. That is,

$$\frac{V_{DC}}{R_L} \geq \frac{4V_m}{3\pi X_L} \quad \text{or} \quad \frac{V_{DC}}{R_L} \geq \left(\frac{2}{3X_L}\right) \times V_{DC} \tag{14.24}$$

This gives,

$$X_L \geq \frac{2R_L}{3} \quad \text{or} \quad L \geq \frac{R_L}{3\omega} \tag{14.25}$$

Therefore,

$$\text{Critical inductance, } L_C = \frac{R_L}{3\omega} \tag{14.26}$$

L_C equals $R_L/942$ for a power line frequency of 50 Hz and $R_L/1131$ for a power line frequency of 60 Hz. Here, R is in ohms and L_C is in henries. In practice, L_C should be about 25% higher to take care of approximation made in writing expression for $V(t)$ as given in Eq. (14.20). This gives $L \geq R_L/754$ (for power line frequency of 50 Hz) and $\geq R_L/905$ (for power line frequency of 60 Hz).

Multiple LC sections can be used to further smoothen the output. Figure 14.12 shows one such filter using two LC sections. The filter can be analyzed in the same fashion as it was done in the case of a single section filter.

$$\text{Ripple factor, } r = \left(\frac{\sqrt{2}}{3}\right) \times \left(\frac{X_{C1}}{X_{L1}}\right) \times \left(\frac{X_{C2}}{X_{L2}}\right) \tag{14.27}$$

For $L_1 = L_2 = L$ and $C_1 = C_2 = C$,

$$r = \frac{\sqrt{2}}{48\omega^4 L^2 C^2} \tag{14.28}$$

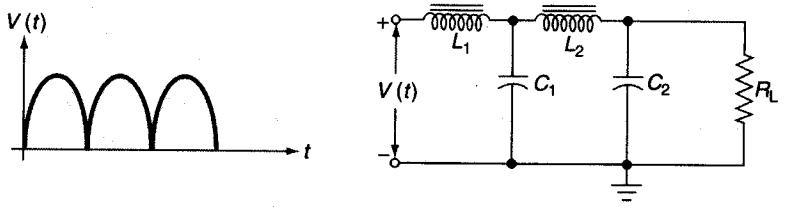


Figure 14.12 | Two-section LC filter with full-wave rectified input.

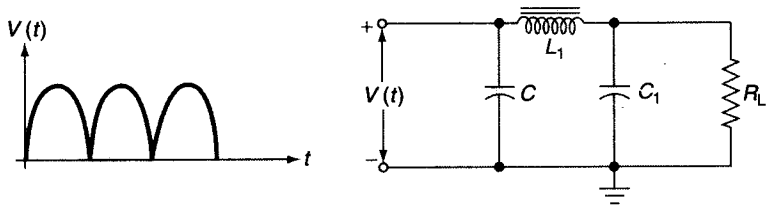


Figure 14.13 | CLC or π-type filter.

Ripple factor equals $3/L^2C^2$ for power line frequency of 50 Hz and $1.45/L^2C^2$ for power line frequency of 60 Hz. Here, L is in henries and C in microfarads. The value of critical inductance is as it is in the case of single section filter.

CLC Filter (π-Filter)

Figure 14.13 shows the CLC filter, which is basically a capacitor filter followed by LC section. The ripple characteristics of this filter are similar to those of two-section LC filter and the expression for ripple factor can be written as

$$\text{Ripple factor, } r = \sqrt{2} \times \left(\frac{X_C}{R_L}\right) \times \left(\frac{X_{C1}}{X_{L1}}\right) \tag{14.29}$$

The circuit however suffers from the problem of high diode peak currents, poor regulation and a ripple that is dependent upon the value of load resistance. In the case of very small load current, one may replace the inductance (L) with a resistance equal in value to the inductive reactance at the ripple frequency of 2ω.

EXAMPLE 14.5

Refer to the voltage waveform of Figure 14.14 observed across the load in the case of a power supply. Determine the ripple factor and percentage ripple content.

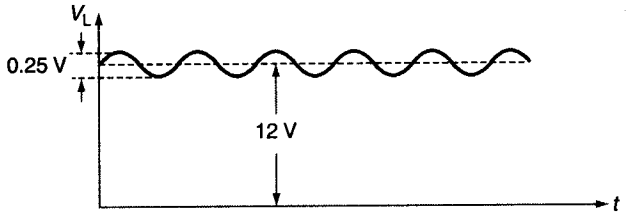


Figure 14.14 | Example 14.5.

Solution

1. From Figure 14.14, $V_{DC} = 12$ V and V_r (peak-to-peak) = 0.25 V.
2. V_r (RMS) = $0.25/2\sqrt{2} = 0.088$ V.
3. Therefore, ripple factor, $r = V_r$ (RMS)$/V_{DC} = 0.088/12 = 0.00737$.
4. Percentage ripple = 0.74%.

EXAMPLE 14.6

A power supply uses a full-wave rectifier and a capacitor filter. The filter feeds a load resistance of 1000 Ω. If the DC voltage across the load is 12 V and the peak-to-peak value of ripple were not to exceed 0.2 V, determine the minimum capacitance value of the filter capacitor. Assume a power line frequency of 50 Hz.

Solution

1. Peak-to-peak ripple voltage, V_r (peak-to-peak) = 0.2 V.
2. The ripple waveform can be assumed to be triangular in shape. Therefore, V_r (RMS) = $0.2/2\sqrt{3} = 0.058$ V.
3. Ripple factor in the case of capacitor filter is given by

$$r = V_r \text{ (RMS)}/V_{DC} = 0.058/12 = 0.0048$$

Therefore, $1/4\sqrt{3}fCR_L = 0.0048$.

4. Substituting the values of R_L and f, we get

$$C = 1/(4\sqrt{3} \times 50 \times 0.0048 \times 1000) = 601 \ \mu\text{F}$$

EXAMPLE 14.7

An LC filter connected at the output of a full-wave rectifier operating at a power line frequency of 50 Hz is required to provide a ripple of 1 percent. It is recommended to have L/C ratio not to exceed 0.005 with L in henries and C in microfarads. Determine the required values of L and C. How would the ripple factor change if an identical LC section were connected in cascade to make it a two-section LC filter?

Solution

1. Ripple factor = $1.2/LC$ for a power line frequency of 50 Hz. In this expression, L is in henries and C is in microfarads.
2. $L/C = 0.005$ where L is in henries and C is in microfarads. This gives $L = 0.005C$.
3. Substituting the value of L in the expression for ripple factor, we get

$$\text{Ripple factor} = 1.2/(C \times 0.005C) = 1.2/0.005C^2 = 0.01$$

4. This gives, $C^2 = 1.2/(0.005 \times 0.01) = 24000$, which gives $C = \sqrt{24000} = 155$ μF.
5. This gives $L = 0.005 \times 155 = 0.775$ henries.
6. In the case of two-section LC filter, ripple factor is given by $r = \sqrt{2}/(48\omega^4 L^2 C^2)$, which reduces to $r = (3/L^2C^2)$ for a power line frequency of 50 Hz. Here, L is in henries and C is in microfarads.
7. Substituting the values of L and C, we get

$$r = 3/[(0.775)^2 \times (155)^2] = 0.0002 = 0.02\%$$

EXAMPLE 14.8

A π-type CLC filter is connected across the output of a full-wave rectifier, which in turn is fed with a 50 Hz sine wave. The filter feeds a load resistance of 1000 Ω. If the desired ripple factor is 0.001 and the two capacitors are 100 μF each, determine the minimum value of inductance needed to get the desired ripple factor. Also determine the value of resistance required to replace the inductor and still produce the same ripple.

Solution

1. Ripple factor in the case of π-type CLC filter is given by
$$r = \sqrt{2} \times (X_C/R_L) \times (X_{C1}/X_{L1})$$
2. $X_C = 1/2\pi fC$ where $f = 100$ Hz because of full-wave rectification.
3. $X_C = 1/(2 \times 3.14 \times 100 \times 100 \times 10^{-6}) = 15.92\ \Omega = X_{C1}$.
4. $R_L = 1000\ \Omega$ and $X_{L1} = 2\pi fL = 628.3\ \Omega$.
5. From the expression of ripple factor,
$X_{L1} = \sqrt{2} \times (X_C/R_L) \times (X_{C1}/r) = 1.414 \times (15.92/1000) \times (15.92/0.001) = 358.4$
Therefore, $L = 358.4/628.3 = 0.57$ henry.
6. Value of resistance required to replace the inductance and still provide the same ripple is equal to the inductive reactance.
7. Therefore, required value of resistance, $R = X_{L1} = 358.4\ \Omega$.

14.5 Linear Regulators

As outlined earlier, the regulator circuit in a power supply ensures that the load voltage (in the case of voltage regulated power supplies) or the load current (in the case of current regulated power supplies) is constant irrespective of variations in the line voltage or load resistance. In the present section are discussed different types of linear voltage regulator circuits. Three basic types of linear voltage regulator configurations include the emitter–follower regulator, series-pass regulator and shunt regulator. Each one of these is briefly described in the following sections.

Emitter–Follower Regulator

Figure 14.15 shows the basic positive output emitter–follower regulator. The emitter voltage, which is also the output voltage, remains constant as long as the base voltage is held constant. A Zener diode connected at the base ensures this. The regulated output voltage in this case is $(V_Z - 0.7)$ V. The emitter–base voltage of the transistor is assumed to be 0.7 V. Another way of explaining the regulation action provided by the

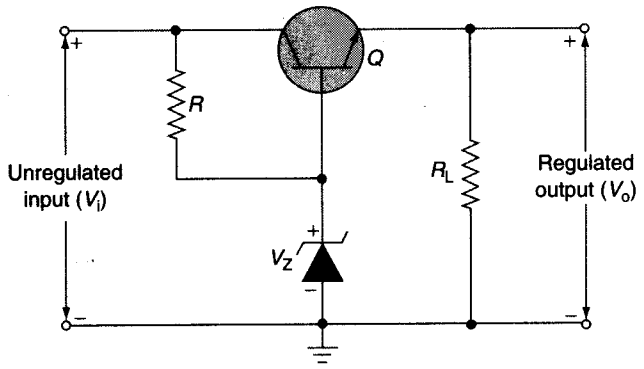


Figure 14.15 | Emitter–follower regulator for positive output voltages.

circuit is as follows. When the output voltage tends to increase, the emitter–base voltage of the series transistor decreases thus decreasing its conduction. This increases collector–emitter drop across the transistor to maintain a constant output voltage. When the output voltage tends to decrease, the emitter–base voltage increases thus increasing the conduction of the transistor. This decreases the collector–emitter drop across the transistor again maintaining a constant output voltage. Owing to high inherent current gain of the series-pass transistor, a low-power Zener diode can be used to regulate high value of load current. The base current in this case needs to be only $[1/(1 + h_{fe})]$ times the load current. Figure 14.16 shows the emitter–follower regulator circuit for negative output voltages. The regulated output voltage in this case is $-(V_Z - 0.7)$ V. If the load current is so large that it is beyond the capability of the Zener diode to provide the requisite base current, a Darlington combination can be used instead of a single transistor series-pass element (Figures 14.17 and 14.18). The regulated output voltages for the Darlington emitter–follower regulators of Figures 14.17 and 14.18 are $(V_Z - 1.4)$ and $-(V_Z - 1.4)$ V, respectively.

Series-Pass Regulator

The emitter–follower regulator circuit discussed in the previous section is also a type of series-pass regulator where the conduction of the series transistor decides the voltage drop across it and hence the output voltage. The Zener diode provides the reference voltage that controls the conduction of the transistor depending

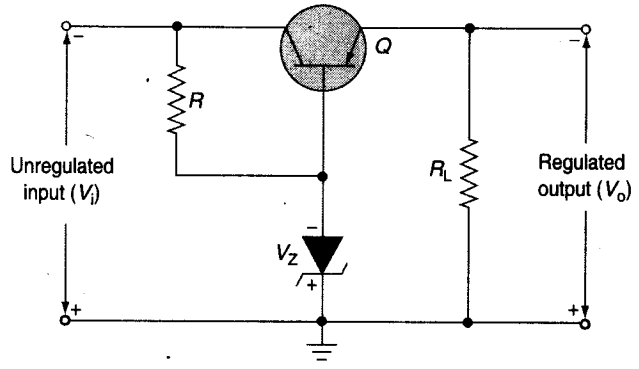


Figure 14.16 | Emitter–follower regulator for negative output voltage.

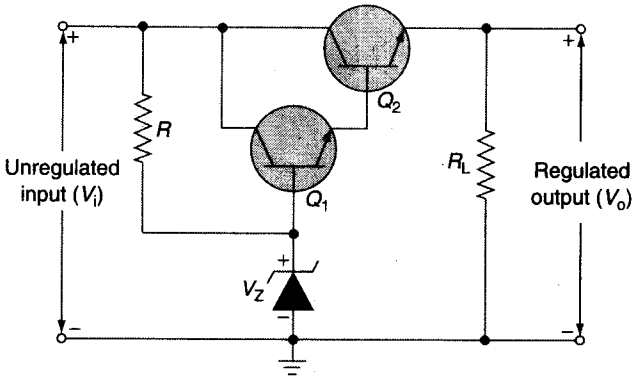


Figure 14.17 | Emitter–follower regulator using Darlington transistor pair (positive output).

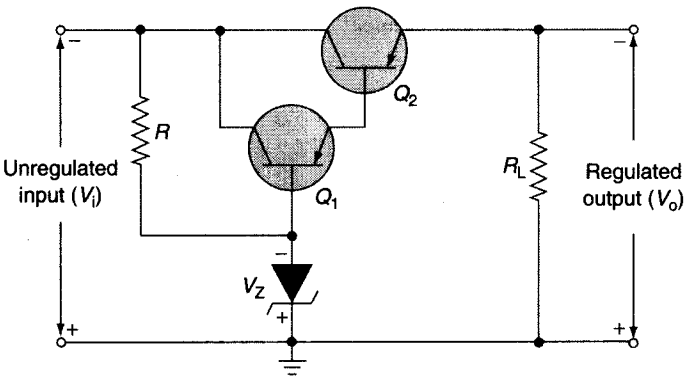


Figure 14.18 | Emitter-follower regulator using Darlington transistor pair (negative output).

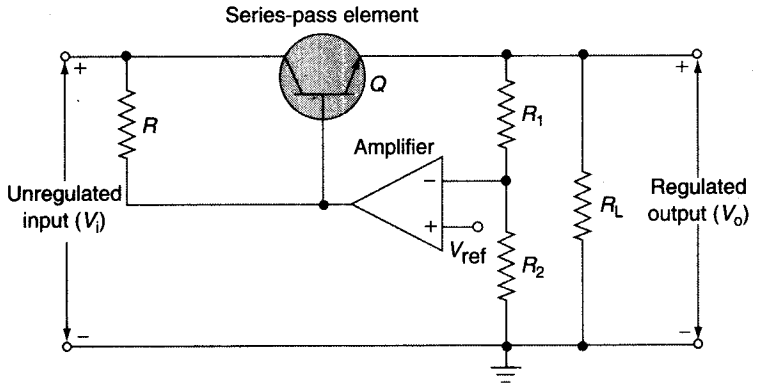


Figure 14.19 | Series-pass linear regulator.

upon the output voltage. Figure 14.19 shows the basic constituents of an improved series-pass-type linear regulator that is capable of providing much better regulation specifications. The series-pass element, a bipolar transistor in the circuit shown, again works like a variable resistance with the conduction of the transistor depending upon the base current. The regulator circuit functions as follows.

A small fraction of the output voltage is compared with a known reference DC voltage and their difference is amplified in a high-gain DC amplifier. The amplified error signal is then fed back to the base of the series-pass transistor to alter its conduction so as to maintain essentially a constant output voltage. The regulated output voltage in this case is given by $V_{ref} \times (R_1 + R_2)/R_2$.

As the output voltage tends to decrease due to decrease in input voltage or increase in load current, the error voltage produced as a result of this causes the base current to increase. The increased base current increases transistor conduction thus reducing its collector–emitter voltage drop, which compensates for the reduction in the output voltage.

Similarly, when the output voltage tends to increase due to increase in input voltage or decrease in load current, the error voltage produced as a consequence is of the opposite sense. It tends to decrease transistor conduction thus increasing its collector–emitter voltage drop again maintaining a constant output voltage. The regulation provided by this circuit depends upon the stability of the reference voltage and the gain of the DC amplifier. A typical series-pass regulator circuit using a bipolar transistor as the error amplifier is

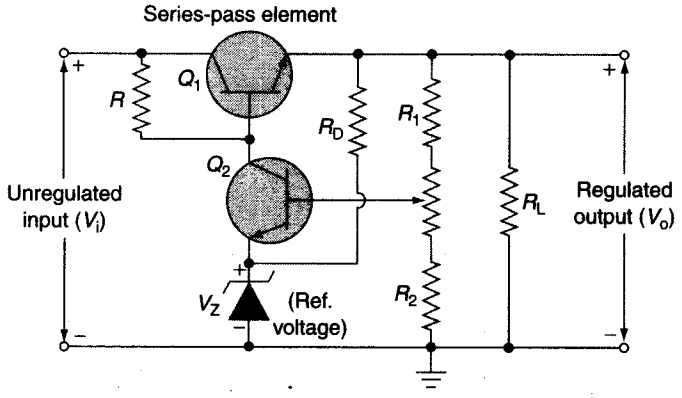


Figure 14.20 | Series-pass linear regulator using bipolar transistor as error amplifier.

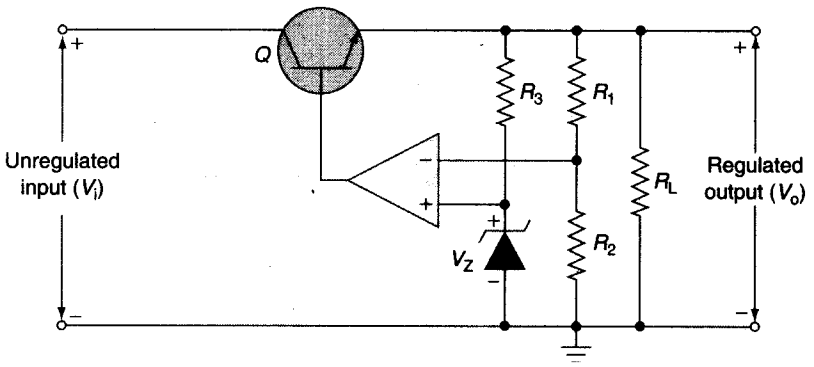


Figure 14.21 | Series-pass linear regulator using opamp-based as error amplifier.

shown in Figure 14.20. Figure 14.21 shows another series-pass regulator circuit that uses an operational amplifier as the error amplifier. The operation of the circuit is similar to that of transistor-based one.

As compared to the emitter–follower type series-pass regulator, the one with an error amplifier in the feedback loop and discussed in this section provides better regulation due to the gain provided by the error amplifier. In this case, given change in output voltage causes a relatively much larger change in the base current of the series-pass element.

Current Limiting

The power dissipated in the series-pass transistor is the product of its collector–emitter voltage and the load current. As the load current increases within a certain range, the collector–emitter voltage decreases due to the feedback action keeping the output voltage as constant. The series-pass transistor is so chosen that it can safely dissipate the power under normal load conditions. If there is an overload condition due to some reason or the other, the transistor is likely to get damaged if such a condition is allowed to persist for long. In the worst case, if there were a short circuit on the output, the whole unregulated input would appear across the series-pass element increasing the power dissipation to prohibitively large magnitude eventually destroying the transistor. Even a series-connected fuse does not help in such a case, as the thermal time constant of the transistor is much smaller than that of the fuse. Thus it is always desirable to build overload protection or current limiting protection in the linearly regulated power supply design. One such configuration is shown in Figure 14.22.

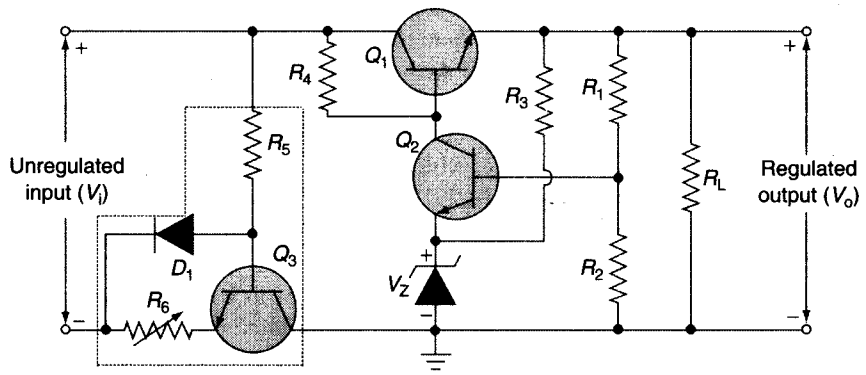


Figure 14.22 | Series-pass linear regulator with overload protection.

Under normal operating conditions, transistor Q_3 is in saturation. Thus, it offers very little resistance to the load current path. In the event of an overload or a short circuit, diode D_1 conducts thus reducing the base drive to transistor Q_3. Transistor Q_3 offers an increased resistance to the flow of load current. In the event of a short circuit, the whole of input voltage would appear across Q_3. Transistor Q_3 should be so chosen that it can safely dissipate power given by the product of worst-case unregulated input voltage and the limiting value of current. Diode D_1 and transistor Q_3 should preferably be mounted on the same heat sink so that emitter–base junction of Q_3 and P–N junction of D_1 are equally affected by temperature rise and the short circuit limiting current is as per the preset value. There can be other possible circuit configurations that can provide the desired protection function.

Figure 14.23 shows another circuit arrangement that provides current-limiting action and overload protection. When the load current is less than the limiting value, the circuit regulates the output voltage normally. Transistor (Q_3) is in cut-off state. As the load current reaches the limiting value, which is determined by resistor R_5, transistor Q_3 conducts and the major part of Q_1 base current gets routed through Q_3, substantially reducing its base drive.

The current-limiting feature described in the previous paragraphs has the advantage of protecting the series-pass transistor and rectifier diodes in the case of any accidental shorting of the output. However, the circuit suffers from the disadvantage of large power dissipation in the series-pass transistor in the event of an output short circuit. The power dissipated in this case is approximately equal to the product of the unregulated input voltage and the limiting value of the load current. A common form of current-limiting feature

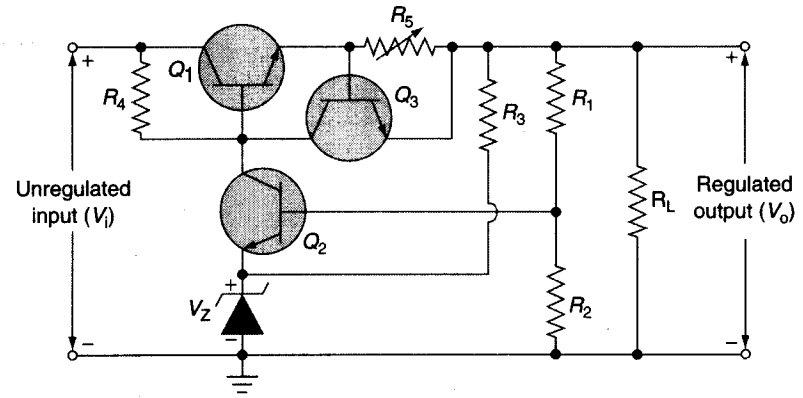


Figure 14.23 | Series-pass linear regulator with overload protection.

practiced in linearly regulated power supplies is the *foldback current limiting*, which overcomes this shortcoming. It is a form of over-current protection where the load current reduces to a small fraction of the limiting value the moment the load current exceeds the limiting value. This helps in drastically reducing the dissipation in series-pass transistor in the case of short circuit condition. Figure 14.24 shows a comparison of voltage versus load current curve in the case of conventional current limiting and foldback current limiting. Figure 14.25 shows the series-pass regulator with foldback current-limiting feature. The circuit is a slight modification of the one shown in Figure 14.23. The base of the current-limiting transistor Q_3 is fed from a potential divider arrangement of R_6 and R_7 instead of being tied to emitter of series-pass transistor Q_1. The circuit of Figure 14.25 functions as follows.

In the event of a short circuit, $V_o = 0$. Therefore, the short-circuit load current (I_{SL}) is the one that produces a voltage equal to V_{BE} required for conduction of current-limiting transistor Q_3. That is,

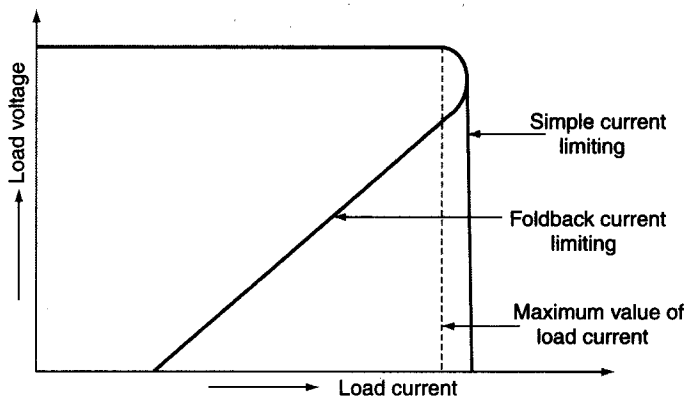


Figure 14.24 | Foldback current limiting.

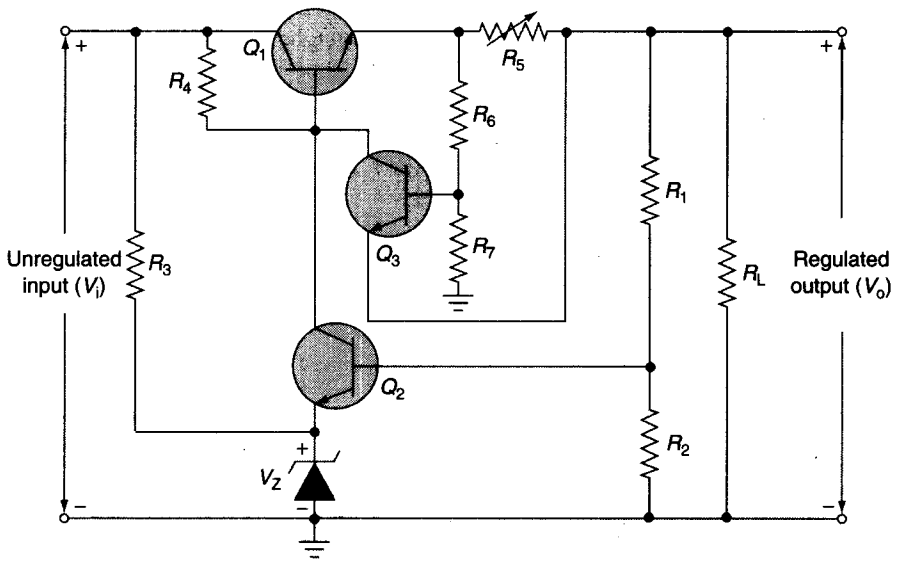


Figure 14.25 | Series regulator with foldback current limiting.

$$V_{BE} = (I_{SL} \times R_5) \times \frac{R_7}{R_6 + R_7} = K \times I_{SL} \times R_5$$

where $K = R_7/(R_6 + R_7)$. This gives

$$I_{SL} = \frac{V_{BE}}{K \times R_5} \tag{14.30}$$

When the output is not shorted, potential of Q_3 emitter terminal is V_o. Therefore, potential of its base terminal (V_{B3}) is given by

$$V_{B3} = V_o + V_{BE} = V_o + K \times I_{SL} \times R_5$$

Potential of the emitter terminal of Q_1 is given by

$$V_{E1} = \frac{V_o + K \times I_{SL} \times R_5}{K} \tag{14.31}$$

Therefore, maximum value of load current (I_{max}) under these conditions is given by

$$I_{max} = \left(\frac{1}{R_5}\right) \times \left[\left\{\frac{(V_o + K \times I_{SL} \times R_5)}{K}\right\} - V_o\right] \tag{14.32}$$

$$I_{max} = \frac{V_o + K \times I_{SL} \times R_5 - V_o \times K}{K \times R_5} \tag{14.33}$$

$$I_{max} = \frac{V_o \times (1-K) + K \times I_{SL} \times R_5}{K \times R_5} \tag{14.34}$$

$$I_{max} = I_{SL} + \left(\frac{V_o \times (1-K)}{K \times R_5}\right) \tag{14.35}$$

Equation (14.35) shows that the maximum load current or the limiting value of the load current is larger than the short-circuit current. Typical value of K is such that the maximum load current is about two to three times the short-circuit load current.

Other types of protection features that are usually built into power supplies include crowbaring and thermal shutdown. Crowbaring is a type of over voltage protection and thermal shutdown disconnects the input to the regulator circuit in the event of temperature of the active device(s) exceeding a certain upper limit. It may be mentioned here that the control and protection functions are usually provided by an integrated circuit (IC) in a modern power supply. A wide range of control ICs is available for both linear and switched mode power supplies.

Shunt Regulator

In a series-type linear regulator, the pass element is connected in series with the load and any decrease or increase in the output voltage is accompanied by a corresponding decrease or increase in the collector–emitter voltage of the series-pass transistor. In the case of a shunt-type linear regulator (Figure 14.26), regulation is provided by a change in the current through the shunt transistor to maintain a constant output voltage. The regulated output voltage in a shunt regulated linear power supply is the unregulated input voltage minus drop across the resistor R_1. Now, the current through R_1 is the sum of load current (I_L) and current through shunt transistor (I_S). As the output voltage tends to decrease, the base current through the transistor reduces with the result that its collector current (I_S) decreases too. This reduces drop across R_1 and the output voltage is restored to its nominal value.

Similarly, the tendency of the output voltage to increase is accompanied by an increase in current through the shunt transistor consequently increasing voltage drop across R_1, which in turn maintains a constant output voltage. A Darlington combination in place of shunt transistor enhances the current capability (Figure 14.27). The regulated output voltages in the case of shunt regulator circuits of Figures 14.26 and 14.27 are $(V_Z + V_{BE})$ and $(V_Z + 2V_{BE})$, respectively. Another shunt regulator configuration is shown in Figure 14.28. In this case, the base terminal of the shunt transistor is driven by the output of an opamp. A reference voltage and the sample of output voltage drive the two inputs of the opamp. If the two voltages differ, the output of opamp forces the shunt element to conduct more or less current through it, thus maintaining a constant output voltage.

Shunt regulator is not as efficient as a series regulator for the simple reason that the current through the series resistor in the case of shunt regulator is the sum of load current and shunt transistor current and it dissipates more power than the series-pass regulator with same unregulated input and regulated output specifications. In a shunt regulator, the shunt transistor also dissipates power in addition to the power dissipated in the series resistor. The only advantage with a shunt regulator is its simplicity and that it is inherently protected against overload conditions.

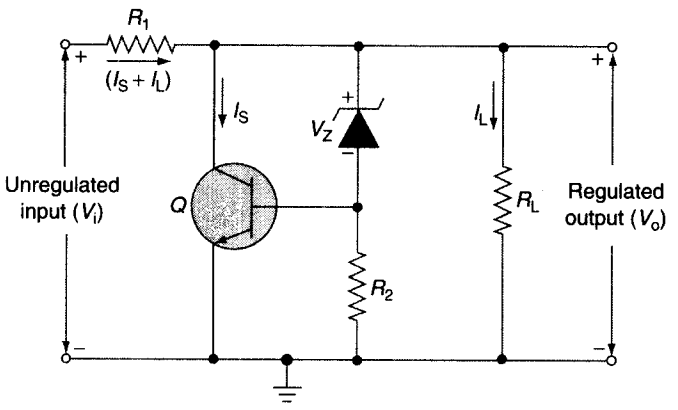


Figure 14.26 | Shunt regulator.

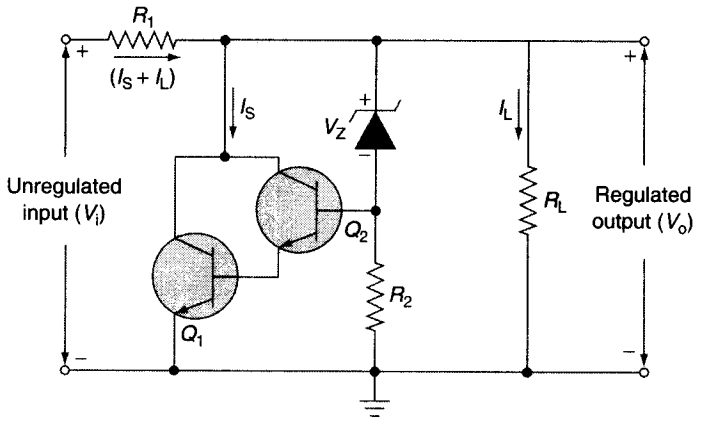


Figure 14.27 | Shunt regulator with Darlington transistor pair.

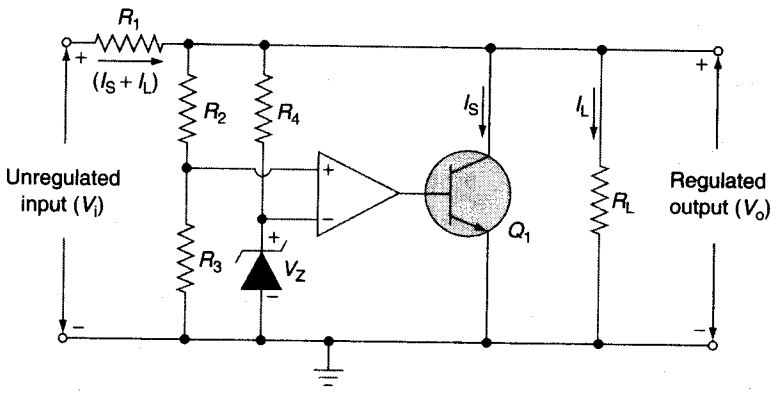


Figure 14.28 | Opamp-based shunt regulator circuit.

EXAMPLE 14.9

Refer to the emitter–follower regulator circuit of Figure 14.29. Determine (a) regulated output voltage; (b) current through the Zener diode. Assume β of the transistor as 50, V_{BE} (Q) = 0.7 V, forward voltage drop of diode D_1 = 0.7 V, Zener diode voltage (V_Z) = 12 V.

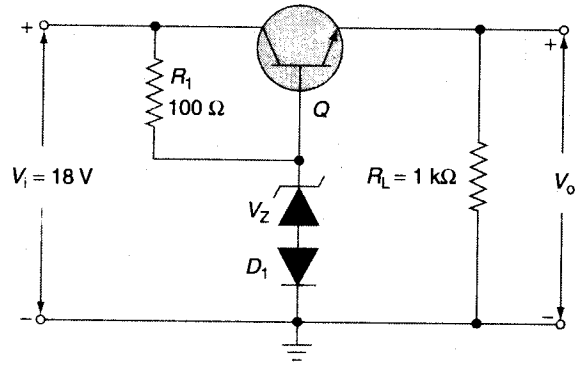


Figure 14.29 | Example 14.9.

Solution

1. Regulated output voltage, $V_o = V_Z + V_{D1} - V_{BE}(Q) = 12 + 0.7 - 0.7 = 12$ V.
2. Therefore, $V_{CE}(Q) = 18 - 12 = 6$ V.
3. Current through resistor $R_1 = (18 - 12.7)/100 = 0.053$ A = 53 mA. Part of this current flows towards the base terminal of Q and the rest flows through the series combination of the Zener diode and diode D_1.
4. Now, load current = 12/1000 = 0.012 A and β of transistor $Q = 50$.
5. Base current of transistor $Q = 0.012/(1 + \beta) = 0.012/51 = 0.24$ mA.
6. Therefore, current through Zener diode = $53 \times 10^{-3} - 0.24 \times 10^{-3} = 52.76$ mA.

EXAMPLE 14.10

Refer to the opamp-based series-pass regulator circuit of Figure 14.30. Determine the regulated output voltage.

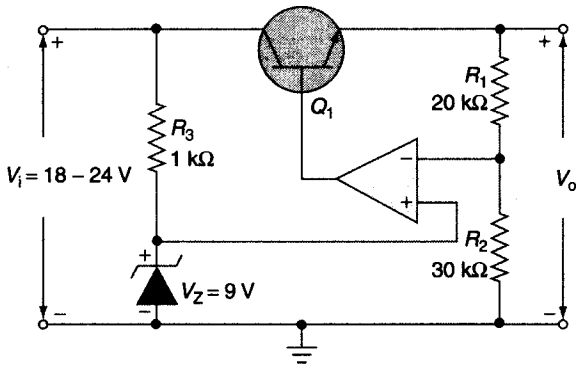


Figure 14.30 | Example 14.10.

Solution

1. The regulated output voltage is the one for which voltage at the inverting input of opamp equals the Zener voltage.
2. That is, $V_o \times 30 \times 10^3/(30 \times 10^3 + 20 \times 10^3) = 9$ or $0.6 \times V_o = 9$.
3. This gives $V_o = 9/0.6 = 15$ V.

EXAMPLE 14.11

For the series-pass regulator circuit of Figure 14.31, determine the range over which the regulated output voltage is adjustable. Assume V_{BE} (Q_2) = 0.7 V.

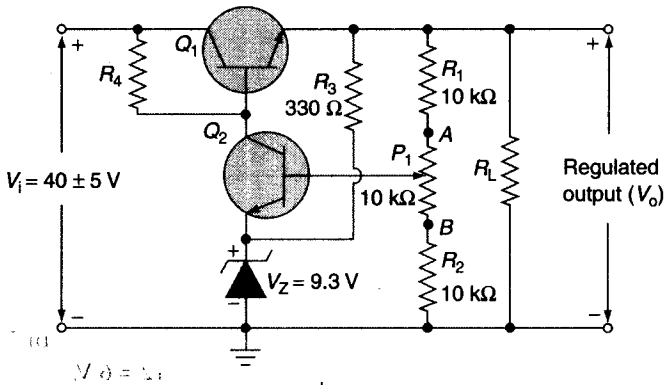


Figure 14.31 | Example 14.11.

Solution

1. Regulated output voltage when the potentiometer P_1 is at position A is given by
$$(9.3 + 0.7) \times [(10 \times 10^3 + 20 \times 10^3)/(20 \times 10^3)] = 15 \text{ V}$$
2. Regulated output voltage when the potentiometer P_1 is at position B is given by
$$(9.3 + 0.7) \times [(10 \times 10^3 + 20 \times 10^3)/(10 \times 10^3)] = 30 \text{ V}$$
3. Therefore, regulated output voltage is adjustable from 15 V to 30 V.

EXAMPLE 14.12

For the basic shunt regulator circuit of Figure 14.32, determine (a) regulated output voltage and (b) maximum power dissipation in resistor R_S. Assume V_{BE} $(Q_1) = 0.7$ V.

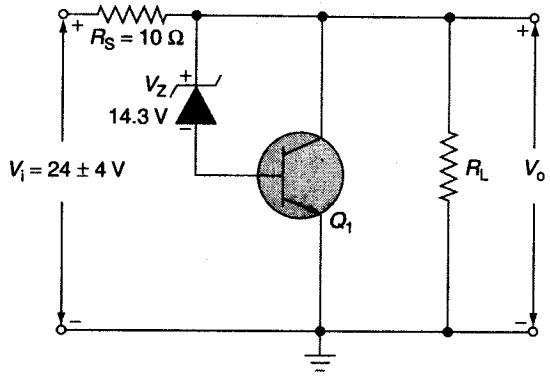


Figure 14.32 | Example 14.12.

Solution

1. Regulated output voltage, $V_o = V_Z + V_{BE}$ $(Q_1) = 14.3 + 0.7 = 15$ V.
2. R_S dissipates maximum power when the unregulated input voltage has maximum value.
3. Now, maximum unregulated input voltage = 28 V.
4. Therefore, maximum power dissipation = $(28 - 15)^2/10 = 16.9$ W.

EXAMPLE 14.13

Refer to the series-pass regulator circuit of Figure 14.33. The regulator circuit has foldback current-limiting feature. Determine (a) regulated output voltage, (b) limiting value of current in the case of short circuit. Assume V_{BE} $(Q_2) = 0.6$ V and V_{BE} $(Q_1) = V_{BE}$ $(Q_3) = 0.7$ V.

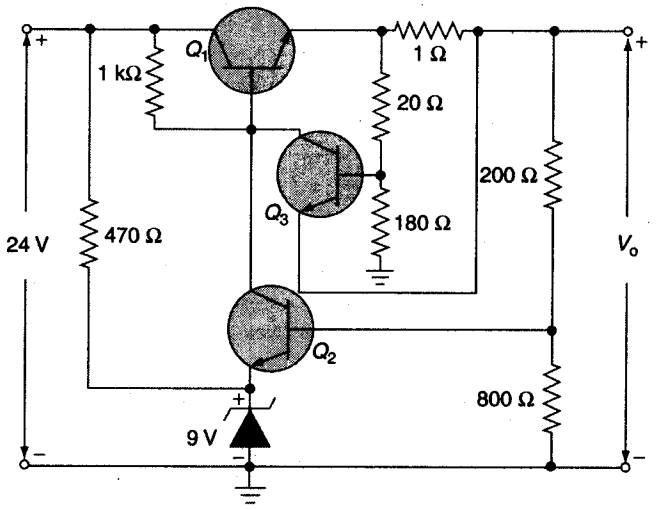


Figure 14.33 | Example 14.13.

Solution

1. Regulated output voltage V_o is given by

$$V_o \times 800/1000 = 9.6$$

Therefore, $V_o = 12$ V.

2. Short-circuit load current = $0.7/0.9 \times 1 = 0.777$ A.
3. Limiting value = $0.777 + [(1 - 0.9) \times 12]/(0.9 \times 1) = 0.777 + 1.2/0.9$

$$= 0.777 + 1.333 = 2.11 \text{ A}$$

14.6 Linear IC Voltage Regulators

Series and shunt regulator circuits designed with discrete components were discussed in the preceding sections. Contemporary regulator circuits are almost exclusively configured around one or more ICs known as IC voltage regulators. IC voltage regulators are available to meet a wide range of requirements. Both fixed output voltage (positive and negative) and adjustable output voltage (positive and negative) IC regulators are commercially available in a wide range of voltage, current and regulation specifications. These have built-in protection features such as current limit, thermal shutdown and so on.

General-Purpose Precision Linear Voltage Regulator

IC 723 is one such general-purpose adjustable output voltage regulator that can be used in positive or negative output power supplies as series, shunt and switching regulator. The internal schematic arrangement of IC 723 resembles the typical circuit for a series-pass linear regulator and comprises a temperature compensated reference, an error amplifier, a series-pass transistor and a current limiter with access to remote shutdown (Figure 14.34).

Figures 14.35 and 14.36 show the basic circuits for building low positive output voltage (2 – 7 V) and high positive output voltage (7 – 37 V) regulator circuits. In the case of the circuit arrangement of Figure 14.35, the regulated output voltage is given by $V_{ref} \times [R_2/(R_1 + R_2)]$. In the case of the circuit arrangement of Figure 14.36, the output voltage is given by $V_{ref} \times [(R_1 + R_2)/R_2]$. In both cases, recommended value of R_3 is $(R_1 \times R_2)/(R_1 + R_2)]$ and $R_{SC} = 0.6/I_{SC}$, where I_{SC} is short-circuit limiting current value.

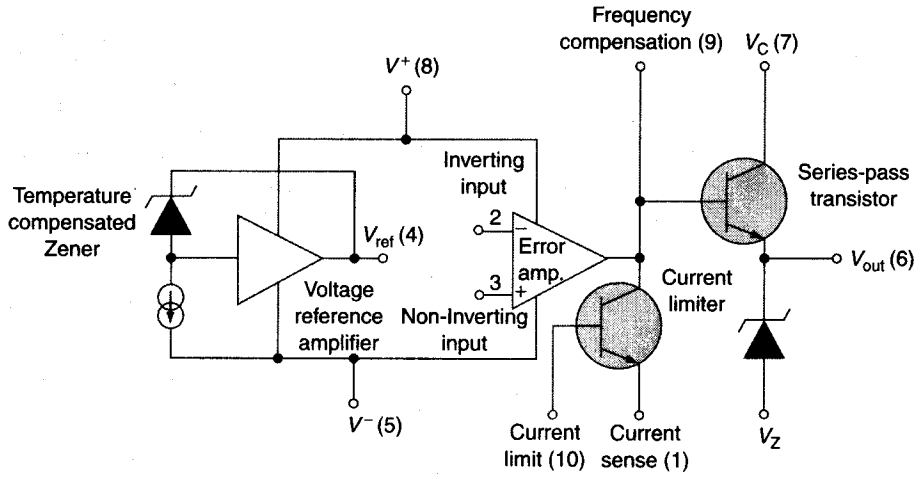


Figure 14.34 | Internal schematic arrangement of IC 723.

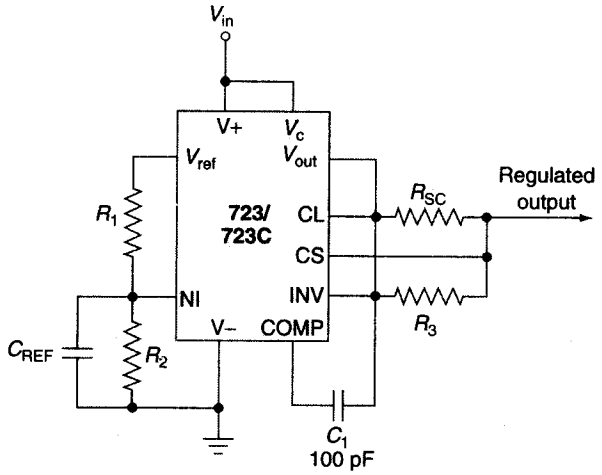


Figure 14.35 | Low positive output voltage regulator using IC 723.

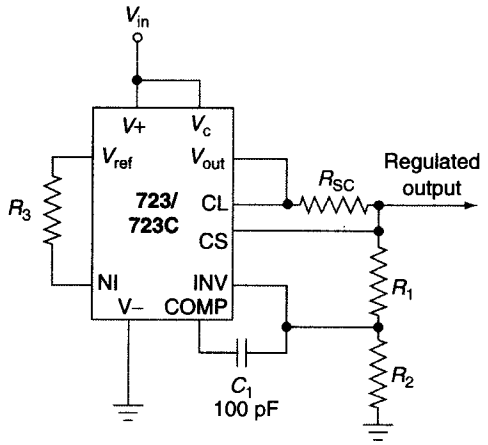


Figure 14.36 | High positive output voltage regulator using IC 723.

Regulator circuits with enhanced load current capability can also be configured around regulator IC 723 with the help of external bipolar transistors. These and many more circuits can be found in application notes of IC 723.

Three-Terminal Regulators

In their basic operational mode, three-terminal regulators require virtually no external components. These are available in both fixed output voltage (positive and negative) as well as adjustable output voltage (positive and negative) types in current ratings of 100 mA, 500 mA, 1.5 A and 3.0 A. Popular fixed positive output voltage types include LM/MC 78XX-series and LM 140XX/340XX-series three-terminal regulators. LM 117/217/317 is a common adjustable positive output voltage regulator type number. Popular fixed negative output voltage types include LM/MC 79XX-series and LM 120XX/320XX-series three-terminal regulators. LM 137/237/337 is a common adjustable negative output voltage regulator type number. A two-digit number in place of "XX" indicates the regulated output voltage. An important specification of three-terminal regulators is

the dropout voltage, which is minimum unregulated input to regulated output differential voltage required for the regulator to produce the intended regulated output voltage. It is in the range of 1.5 V to 3 V and is lower for regulators with lower load current delivery capability and lower regulated output voltage value. For example, a 5 V regulator has a dropout voltage specification of 2 V against 3 V for a 24 V regulator for the same current delivery capability. Also, a 100 mA output regulator has a drop voltage specification of 1.7 V against 3 V for 1500 mA regulator for the same regulated output voltage.

Figure 14.37 shows the basic application circuits using LM/MC 78XX-series and LM/MC 79XX-series three-terminal regulators. Here C_1 and C_2 are decoupling capacitors. C_1 is generally used when the regulator is located far from the power supply filter. Typically, a 0.22 μF ceramic disc capacitor is used for C_1. Capacitor C_2 is typically a 0.1 μF ceramic disc capacitor. LM 140XX/340XX-series and LM 120XX/320XX-series regulators are also used in the same manner. In the case of fixed output voltage three-terminal regulators, if the common terminal instead of being grounded were applied a DC voltage, the regulated output voltage in that case would be greater than the expected value by a quantum equal to the voltage applied to the common terminal.

Figure 14.38 shows the application of fixed output three-terminal regulator as a constant current source. The load current in this case is given by $V_{ref}/R + I_Q$, where I_Q is the quiescent current, typically 8 mA for 78XX-series regulators. For details on the features and facilities of three-terminal regulators and their application circuits, one can refer to data sheets and application notes provided by manufacturers of these devices.

LM 117/217/317 is an adjustable output three-terminal positive output voltage regulator and is available in current ratings of 500 mA, 1000 mA and 1500 mA. The output voltage is adjustable from 1.2 V to 37 V. In the high-voltage version of this series of regulators, designated as LM 117HV/217HV/317HV, the output voltage is adjustable from 1.2 V to 57 V. Figure 14.39 shows the application of LM 117/217/317 as an adjustable regulator.

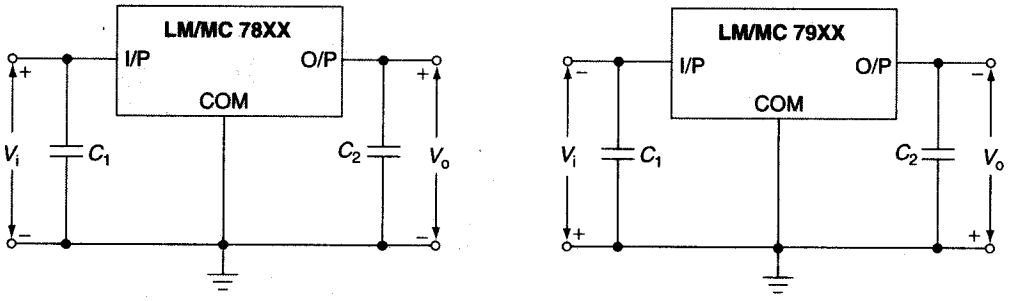


Figure 14.37 | Basic application circuits using three-terminal regulators.

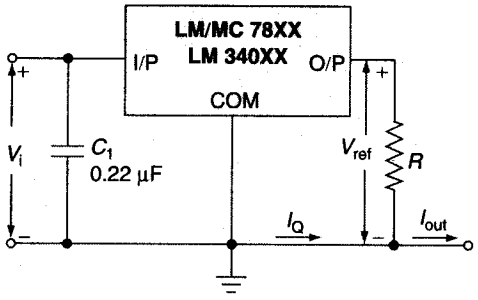


Figure 14.38 | Three-terminal regulator as a constant current source.

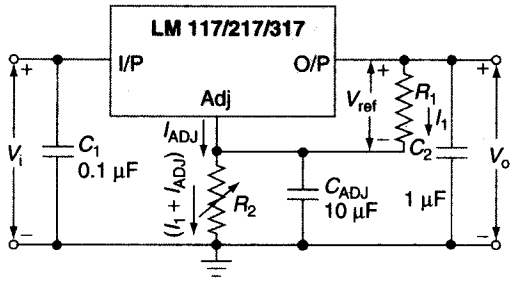


Figure 14.39 Basic application circuit using LM 117/217/317.

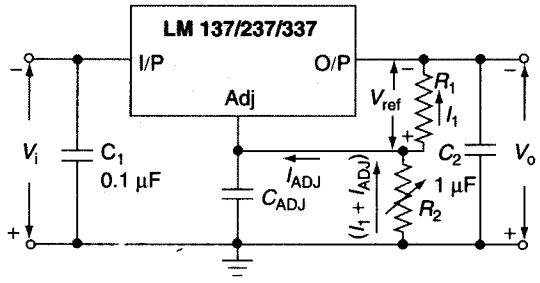


Figure 14.40 Basic application circuit using LM 137/237/337.

Here C_1 and C_2 are decoupling capacitors; C_{ADJ} provides ripple rejection. C_{ADJ} of 10 μF provides typically 80 dB rejection. The output voltage is given by Eq. (14.36):

$$V_o = V_{ref} + \left[\left(\frac{V_{ref}}{R_1}\right) + I_{ADJ}\right] \times R_2 \tag{14.36}$$

$$V_o = \left[\left\{V_{ref} \times \left(\frac{R_1 + R_2}{R_1}\right)\right\} + I_{ADJ} \times R_2\right] \tag{14.37}$$

V_{ref} and I_{ADJ} are typically 1.25 V and 100 μA, respectively.

LM 137/237/337 is an adjustable output three-terminal negative output voltage regulator and is available in current ratings of 500 mA, 1000 mA and 1500 mA. The output voltage is adjustable from −1.2 V to −37 V. In the high-voltage version of this series of regulators, designated as LM 117HV/217HV/317HV, the output voltage is adjustable from −1.2 V to −47 V. Figure 14.40 shows the application of LM 137/237/337 as an adjustable regulator. Here C_1 and C_2 are decoupling capacitors; C_{ADJ} provides ripple rejection. C_{ADJ} of 10 μF provides typically 80 dB rejection. The output voltage is given by

$$V_o = -\left[\left\{V_{ref} \times \left(\frac{R_1 + R_2}{R_1}\right)\right\} + I_{ADJ} \times R_2\right] \tag{14.38}$$

Here V_{ref} and I_{ADJ} are typically −1.25 V and 100 μA, respectively.

Boosting Current Delivery Capability

The load current delivery capability of three-terminal regulators can be increased to more than what they can deliver for a given unregulated input to regulated output voltage differential by using an external transistor. It may be mentioned here that the power dissipated in the regulator is the product of load current and input–output differential voltage. As the power dissipation increases beyond the rated value, the regulator usually goes to thermal shutdown mode. In this mode, the internal series-pass transistor becomes non-conducting, thus allowing the device to cool down.

Figure 14.41(a) shows the typical circuit where an external transistor is used to boost the load current delivery capability of the regulator. In this case, as long as V_{BE} (Q_1) remains below its cut-in voltage, the

regulator functions in its usual manner as if there were no external transistor. As the V_{BE} (Q_1) attains the cut-in voltage due to an increasing load current, Q_1 conducts and bypasses part of load current through it. In fact, the magnitude of load current allowed to go through the regulator equals V_{BE}/R. Rest of the current passes through the external transistor. An NPN transistor can be used to do the job in the case of negative output voltage regulators as shown in Figure 14.41(b).

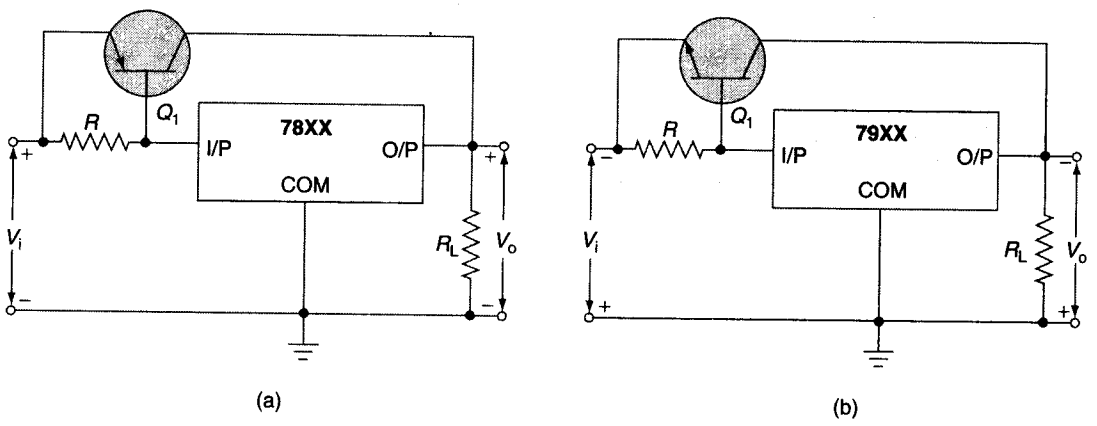


Figure 14.41 | Use of external transistor to boost current delivery capability.

EXAMPLE 14.14

Refer to the three-terminal regulator circuits of Figures 14.42(a) and (b). Determine the regulated output voltages in the two cases given that $V_Z = 3.3$ V and $V_{D1} = 0.7$ V.

Solution

1. For the circuit of Figure 14.42(a)
$$V_o = 5 + V_Z + V_{D1} = 5 + 3.3 + 0.7 = 9 \text{ V}$$
2. For the circuit of Figure 14.42(b)
$$V_o = -12 - V_{D1} = -(12 + 0.7) = -12.7 \text{ V}$$

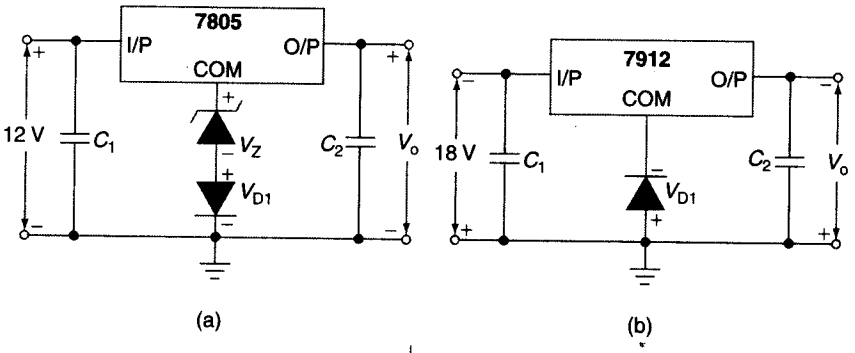


Figure 14.42 | Example 14.14.

EXAMPLE 14.15

Determine the regulated output voltage for the regulator circuit of Figure 14.43 given $V_{ref} = 1.25$ *V.*

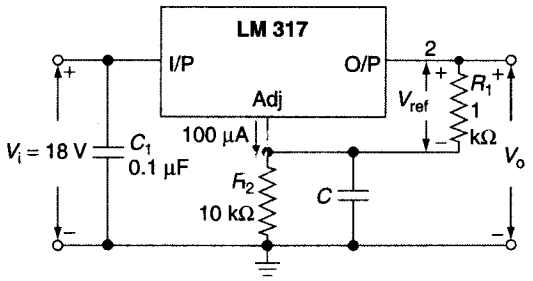


Figure 14.43 | Example 14.15.

Solution

1. The regulated output voltage is sum of voltages across resistors R_1 and R_2. It is given by

$$V_o = V_{ref} + \left[\left(\frac{V_{ref}}{R_1}\right) + I_{ADJ}\right] \times R_2$$

2. Substituting the values, we get

$$V_o = 1.25 + [(1.25/10^3) + 10^{-4}] \times 10 \times 10^3 = 14.75 \text{ V}$$

EXAMPLE 14.16

Using IC voltage regulator-type number LM 7812, design a circuit that generates a variable output voltage adjustable from +15 V to +20 V from an unregulated input of +24 V. Assume quiescent current to be negligible.

Solution

1. Figure 14.44 shows the basic circuit configuration. The output voltage V_o in this case is given by

$$V_o = 12 + [V_o \times R_2/(R_1 + R_2)]$$

$$V_o \times [1 - R_2/(R_1 + R_2)] = 12$$

$$V_o = 12 \times [1 + R_2/R_1]$$

2. V_o (min) = 15 = 12 × [1 + R_2/R_1], which gives R_2 (min) = $R_1/4$.

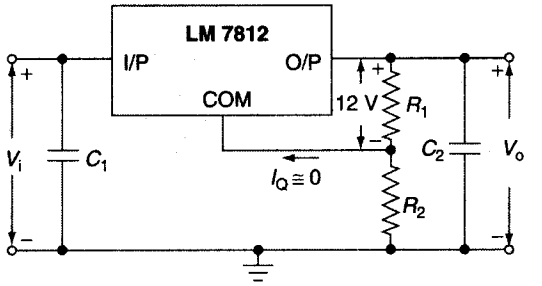


Figure 14.44 | Example 14.16.

3. V_o (max) = 20 = 12 × [1 + R_2/R_1], which gives R_2 (max) = $2R_1/3$.
4. Assuming R_1 = 47 kΩ, R_2 (min) = 11.75 kΩ and R_2 (max) = 31.3 kΩ.
5. C_1 and C_2 are decoupling capacitors and can be 0.1 μF ceramic disks each.

14.7 Regulated Power Supply Parameters

The characteristic parameters that define the quality of a regulated power supply include load regulation, line or source regulation, output impedance or resistance and ripple rejection factor. Each one of these is briefly described in the following paragraphs.

Load Regulation

Load regulation is defined as change in regulated output voltage of the power supply as the load current varies from zero (no-load condition) to maximum rated value (full-load condition). It is usually expressed as a percentage of full-load voltage. That is

$$\text{Percentage load regulation} = \left[\frac{V_{NL} - V_{FL}}{V_{FL}}\right] \times 100 \tag{14.39}$$

Since $V_{FL} \cong V_{NL}$, load regulation may be expressed as a percentage of no-load voltage.

Line Regulation

Line regulation is defined in terms of variation of regulated output voltage for a specified change in line voltage. It is usually expressed as percentage of nominal regulated output voltage. As an example, if the nominal regulated output voltage of 10 V varies by ±1% for a specified variation in line voltage, line regulation in that case would be (0.2/10) × 100 = 2%.

Output Impedance

Output impedance is an important parameter of a regulated power supply. It determines the load regulation of the power supply. The regulated power supply may be represented by a Thevenin's equivalent circuit comprising a voltage source equal to the open circuit voltage across power supply output terminals in series with impedance equal to the output impedance of the power supply. The voltage appearing across the load resistance is equal to the open circuit voltage minus drop across output impedance of the power supply. The voltage drop increases with increase in load current resulting in reduction of voltage across the load. Another way of explaining the same is that the output impedance of the power supply and the load resistance form a potential divider. The load voltage decreases with decrease in load resistance value. An ideal power supply has an output impedance of zero, which renders the output voltage independent of the load resistance value.

Practical power supplies very nearly approach the ideal condition because of emitter–follower nature of regulator circuit characterized by low output impedance, which is further reduced by a factor of (1 + loop gain) due to voltage feedback. Loop gain is the product of output voltage feedback factor and the gain of the error amplifier. Output impedance is typically of the order of few milli-ohms.

Ripple Rejection Factor

Ripple rejection factor is defined as the ratio of ripple in the regulated output voltage to the ripple present in unregulated input voltage. That is

$$\text{Ripple rejection factor} = \frac{V_{RIPPLE}\,(\text{output})}{V_{RIPPLE}\,(\text{input})} \tag{14.40}$$

When expressed in decibels, ripple rejection equals

$$20\log\left[\frac{V_{RIPPLE}(\text{output})}{V_{RIPPLE}(\text{input})}\right]\text{dB}$$

Ripple in unregulated input is nothing but a periodic variation in input voltage. It manifests at the output with a reduced value. Again, the factor by which ripple is reduced equals the de-sensitivity factor (1 + loop gain) due to negative feedback. That is

$$V_{RIPPLE}(\text{output}) = \frac{V_{RIPPLE}(\text{input})}{1 + \text{Loop gain}}$$

EXAMPLE 14.17

A regulated power supply operates from 220 ± 20 VAC. It produces a no-load regulated output voltage of 24 ± 0.5 VDC. Also, the regulated output voltage falls from 24 VDC to 23.8 VDC as the load changes from no-load to full-load condition for the nominal value of input voltage. Determine (a) line regulation and (b) load regulation.

Solution

1. Line regulation = (24.5 − 23.5)/24 = 1/24 = 0.0417 = 4.17%
2. Load regulation = (24 − 23.8)/23.8 = 0.2/23.8 = 0.0084 = 0.84%

EXAMPLE 14.18

A regulated power supply provides a ripple rejection of −80 dB. If the ripple voltage in the unregulated input were 2 V, determine the output ripple.

Solution

1. Ripple rejection in dB is given by

$$20\log\left[\frac{\text{Output ripple}}{\text{Input ripple}}\right] = -80\text{ dB}$$

2. Therefore,

$$\log\left[\frac{\text{Output ripple}}{\text{Input ripple}}\right] = -4$$

$$\frac{\text{Output ripple}}{\text{Input ripple}} = 10^{-4}$$

3. Therefore, output ripple = 2×10^{-4} V = 0.2 mV.

EXAMPLE 14.19

Figure 14.45 shows load voltage versus load current characteristics of a regulated power supply. Determine the output impedance of the power supply.

Solution

1. Output impedance is given by ratio of change in output voltage for known change in load current.
2. From the given characteristic curve, output impedance = (24 − 23.5)/(10 − 0) = 0.5/10 = 0.05 Ω = 50 mΩ.

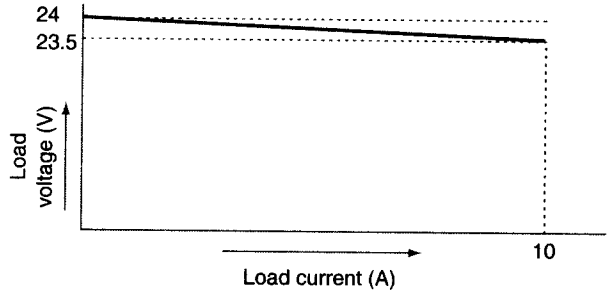


Figure 14.45 | Example 14.19.

EXAMPLE 14.20

Refer to the three-terminal regulator circuit of Figure 14.46. Determine (a) load current; (b) current through LM 7812; (c) current through external transistor; (d) power dissipated in LM 7812. Take V_{BE} $(Q_1) = 0.7$ *V.*

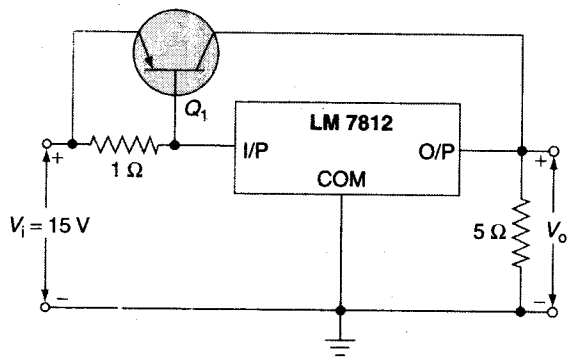


Figure 14.46 | Example 14.20.

Solution

1. Load current = 12/5 = 2.4 A.
2. Current through regulator = 0.7/1 = 0.7 A.
3. Current through external transistor = 2.4 – 0.7 = 1.7 A.
4. Voltage appearing at regulator input = 15 – 0.7 = 14.3 V.
5. Therefore power dissipated in the regulator = (14.3 – 12) × 0.7 = 1.61 W.

KEY TERMS

Emitter–follower regulator
Filter circuit
Line regulation
Load regulation
Output impedance
Peak inverse voltage
Ratio of rectification
Rectifier circuit
Regulator circuit
Ripple factor
Ripple frequency
Ripple rejection factor
Series-pass linear regulator
Shunt regulator
Three-terminal regulator
Transformer
Transformer utilization factor

OBJECTIVE-TYPE EXERCISES

Multiple-Choice Questions

1. The no load and rated load output voltages in a regulated power supply are the same. Its output impedance is therefore
   a. extremely small.
   b. zero.
   c. infinite.
   d. extremely large.

2. Which of the following filter types is suitable only for large values of load resistance?
   a. Capacitor filter
   b. Inductor filter
   c. Choke-input filter
   d. π-type CLC filter

3. Which of the following filter types is suitable only for small values of load resistance?
   a. Capacitor filter
   b. Inductor filter
   c. Choke-input filter
   d. π-type CLC filter

4. Identify the wrong expression.
   a. TUF = DC power delivered to load/AC rating of transformer secondary
   b. Load regulation = [V_o (No load) − V_o (Full load)]/V_o (No load)
   c. Ratio of rectification = DC power delivered to load/AC power available across transformer secondary
   d. Ripple factor = RMS value of AC component/DC value of the rectified wave

5. If the transformer utilization factor for a particular rectifier configuration is small, it implies that
   a. for a given transformer rating, it would deliver a larger DC power to the load.
   b. for a given transformer rating, it would deliver lesser DC power to the load.
   c. the ratio of DC power delivered to the load to the AC power available at the input of rectifier circuit from transformer secondary is small.
   d. none of these.

6. Mark the rectifier circuit that has the least ripple.
   a. Half-wave rectifier
   b. Two-diode full-wave rectifier with center tapped secondary
   c. Bridge rectifier
   d. Both (b) and (c)

7. Which of the characteristic curves shown in Figure 14.47 is for linear power supply with foldback current limiting?
   a. Figure 14.47(a)
   b. Figure 14.47(b)
   c. Figure 14.47(c)
   d. Figure 14.47(d)

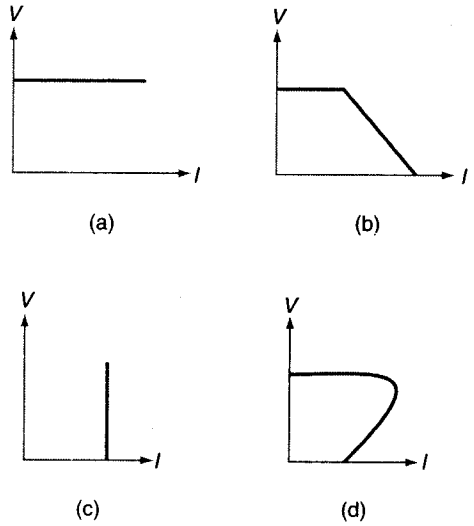


Figure 14.47 | Multiple-choice question 7.

8. In a series-pass linear regulator, voltage drop across series-pass element
   a. is independent of changes in output voltage.
   b. changes directly with changes in output voltage.
   c. changes inversely with changes in output voltage
   d. none of these.

9. The type of linear voltage regulator that is inherently immune to overload condition is
   a. emitter–follower regulator.
   b. series-pass regulator with error amplifier in feedback loop.
   c. shunt regulator.
   d. none of these.

10. In a series-pass linearly regulated power supply, regulated output voltage is 12 V across a load resistance of 1.2 kΩ. The unregulated input is 18 ± 3 V. The worst case power dissipation in the series-pass element would be
   a. 0.09 W
   b. 0.9 W
   c. 0.05 W
   d. 0.21 W

11. A voltage regulator provides a ripple rejection of −60 dB. If the ripple in the unregulated input were 0.5 V, the ripple in the regulated output would be
   a. 0.5 mV
   b. 60 mV
   c. 1 mV
   d. 5 mV

12. Voltage regulators use
   a. positive feedback.
   b. negative feedback.
   c. either positive or negative feedback.
   d. no feedback.

13. IC 7912 produces a regulated output voltage of
   a. +12 V
   b. −12 V
   c. 0 to +12 V
   d. 0 to −12 V

14. Which of the following IC voltage regulators is an adjustable negative output voltage regulator.
   a. LM 317
   b. LM 117
   c. LM 217
   d. LM 237

15. In the case of foldback current limiting, the short circuit load current is
   a. less than the maximum possible load current.
   b. more than the maximum possible load current.
   c. equal to the maximum possible load current.
   d. zero.

Determine the Output

Refer to the regulator circuits of Figure 14.48(a)–(d). Determine the output voltage in each of the four circuits given that V_{BE} of transistors and the forward-biased diode voltage drop in different circuits is 0.7 V.

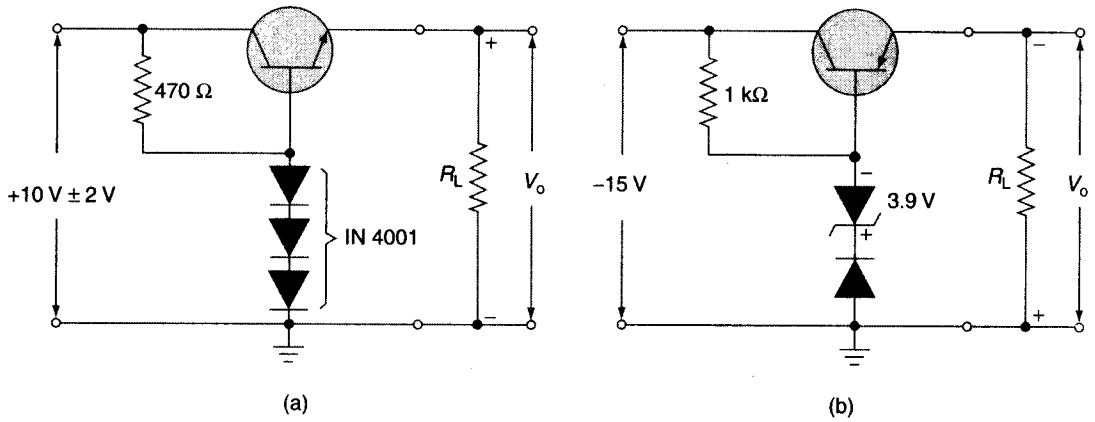


Figure 14.48 | Regulator circuits.

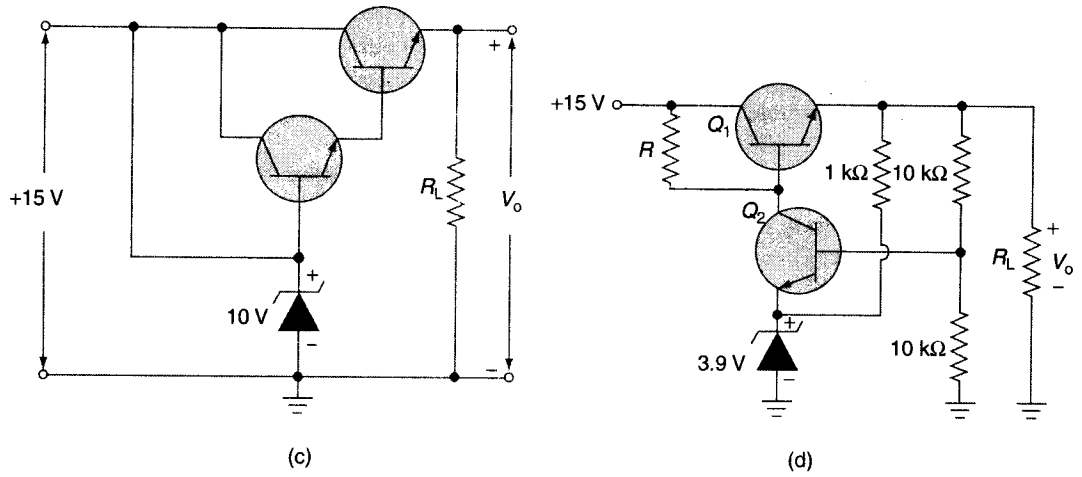


Figure 14.48 | *Continued.*

REVIEW QUESTIONS

1. Name the constituent parts of a basic linearly regulated power supply. Briefly describe the function of each of the constituent parts.

2. Define the following parameters with reference to rectifier circuits. Also write expressions for these parameters in the case of half-wave, conventional full-wave with center-tapped secondary and bridge rectifier circuits.
   a. Ripple frequency
   b. Ratio of rectification
   c. Transformer utilization factor

3. Draw the basic circuit configurations in the case of following types of rectifier circuits.
   a. Conventional full-wave rectifier for negative output voltage
   b. Bridge rectifier for positive output voltage
   c. Half-wave rectifier for negative output voltage

   What is the minimum required peak inverse voltage rating of the diodes used in these rectifier circuits?

4. Give reasons for the following.
   a. Why inductor filter is suitable only for low values of load resistance?
   b. Why capacitor filter is suitable only for high values of load resistance?
   c. Why shunt regulator is not adversely affected by overload condition?
   d. Why is shunt regulator less efficient than a series-pass regulator?

5. Briefly describe the operational principle of an emitter–follower regulator. Draw the basic circuit configurations of positive output and negative output emitter–follower regulators.

6. With the help of basic circuit configuration, briefly describe the operational principle of a shunt regulator.

7. Define load regulation, line regulation, output impedance and ripple rejection factor with reference to regulated power supplies. What decides ripple rejection offered by a regulator circuit?

8. What is current limiting in regulated power supplies? How does foldback current limiting differ from conventional current limiting? What is the advantage of using foldback current limiting over conventional current limiting?
9. With the help of circuit diagram, explain how the load current delivery capability of positive and negative output three-terminal regulators can be enhanced with the help of externally connected bipolar transistors.
10. With the help of circuit diagrams, briefly explain how
    a. Fixed output voltage three-terminal regulator can be used to get a variable regulated output.
    b. A 12 V output three-terminal regulator can be used to get a 15 V regulated output.
    c. A −5 V output three-terminal regulator can be used to get −5.6 V output.
    d. A three-terminal regulator can be used as a constant current source.

PROBLEMS

1. Given that ripple factor in the case of a full-wave rectifier is 0.482, determine the ratio-of-rectification for the same.
2. Determine the transformer rating if it were to deliver a DC power of 1000 W to a resistive load using a bridge rectifier given that the transformer utilization factor in the case of bridge rectifier is 0.812.
3. If ripple factor and ratio-of-rectification are respectively designated as r and R, prove that $r = \sqrt{(1-R)/R}$.
4. A power supply uses a bridge rectifier and a capacitor filter. The filter feeds a load resistance of 500 Ω. If the DC voltage across the load is 12 V and the peak-to-peak value of ripple were not to exceed 0.1 V, determine the minimum capacitance value of the filter capacitor. Assume a power line frequency of 50 Hz.
5. A π-type CLC filter is connected across the output of a bridge rectifier, which in turn is fed with a 50 Hz sine wave. The filter feeds a load resistance of 1 kΩ. If the desired ripple factor is 0.002 and the two capacitors are 47 μF each, determine the minimum value of inductance needed to get the desired ripple factor. Also determine the value of resistance required to replace the inductor and still produce the same ripple.
6. Figure 14.49 shows the basic emitter–follower type of voltage regulator circuit. If the Zener diode is to be biased at least at 10 mA at all times, determine (a) regulated output voltage; (b) value of R given that transistor β is equal to 100 and $V_{BE} = 0.7$ V.

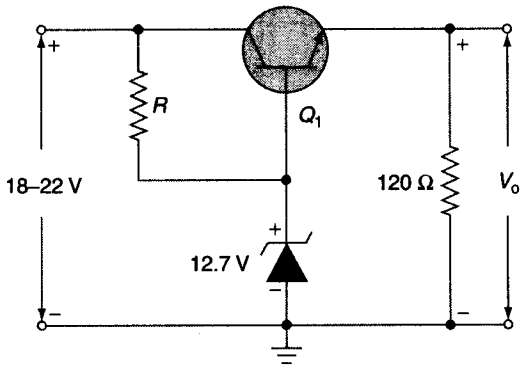


Figure 14.49 | Problem 6.

7. Find the regulated output voltage (V_o) for the emitter–follower regulator circuit of Figure 14.50. Also determine the current (I_Z) if transistors Q_1 and Q_2 in the Darlington pair have β of 10 and 100, respectively. (Given that the forward voltage drop of diodes D_1 and D_2 is 0.6 V, $V_{BE}(Q_1) = 0.6$ V and $V_{BE}(Q_2) = 0.6$ V.
8. The output voltage of a regulated power supply drops by 1 V from no load to rated full load of 1 A. If the no load output voltage is 24 V, determine load regulation and output impedance of the power supply.

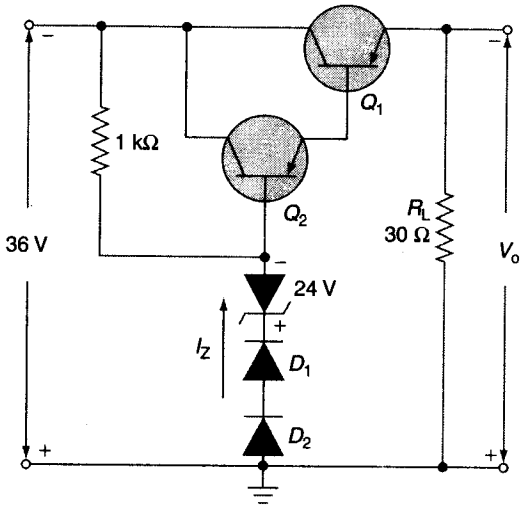


Figure 14.50 | Problem 7.

9. Refer to the series-pass regulator circuit of Figure 14.51. Determine the minimum and maximum possible regulated output voltages. Also determine the maximum power dissipated in transistor Q_1. Assume $V_{BE}(Q_1) = V_{BE}(Q_2) = V_{BE}(Q_3) = 0.6$ V.

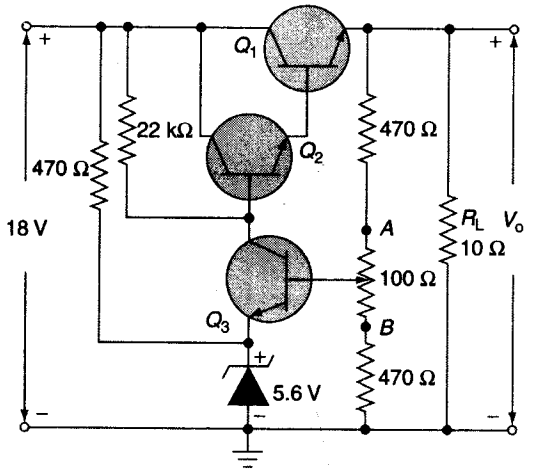


Figure 14.51 | Problem 9.

10. Refer to the three-terminal regulator circuit of Figure 14.52 using an external current boost transistor Q. Determine the power dissipated in regulator 7812. What is the power dissipated if the load resistance were reduced to 10 Ω? Assume $V_{BE}(Q) = 0.6$ V.

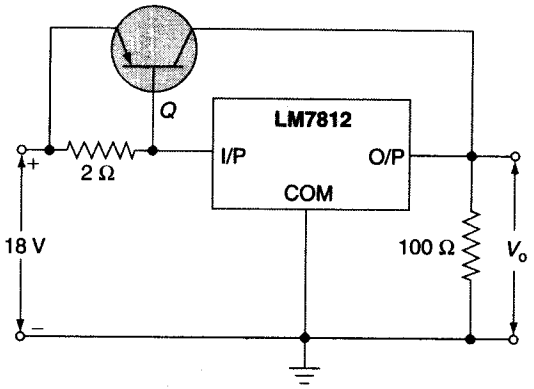


Figure 14.52 | Problem 10.

11. Refer to the three-terminal regulator circuit of Figure 14.53. Determine the regulated output voltage and power dissipated in the regulator.

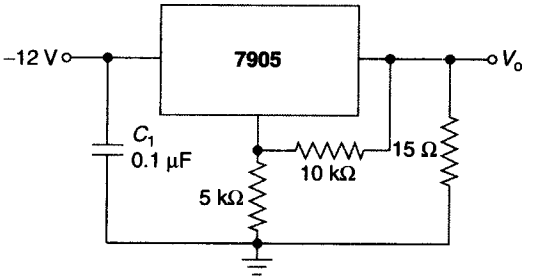


Figure 14.53 | Problem 11.

12. In the case of LM 317-based regulator circuit of Figure 14.54, determine (a) regulated output voltage with the variable resistance at its minimum value and voltage applied to the base terminal of transistor Q is 0 V; (b) regulated output voltage with the variable resistance at its maximum value and voltage applied to the base terminal of Q is 0 V; (c) regulated output voltage with the variable resistance at its minimum value and voltage applied to the base terminal of transistor Q is 5 V and (d) regulated output voltage with the variable resistance at its maximum value and voltage applied to the base terminal of transistor Q is 5 V. V_{ref} of LM 317 = 1.25 V.

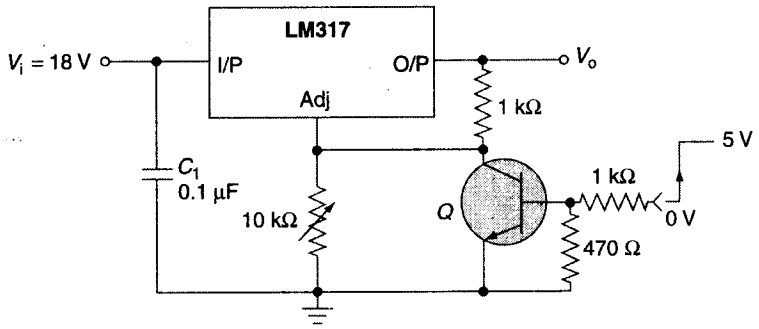


Figure 14.54 | Problem 12.

ANSWERS

Multiple-Choice Questions

1. (b)	**4.** (b)	**7.** (d)	**10** (a)	**13.** (b)
2. (a)	**5.** (b)	**8.** (b)	**11.** (a)	**14.** (d)
3. (b)	**6.** (d)	**9.** (c)	**12.** (b)	**15.** (a)

Determine the Output

Figure 14.48(a): 1.4 V

Figure 14.48(b): −3.9 V

Figure 14.48(c): 8.6 V

Figure 14.48(d): 9.2 V

Problems

1. 0.812

2. 1233.7 W

4. 2400 μF

5. 0.645 henry, 405.3 Ω

6. (a) 12 V, (b) 524.75 Ω

7. $V_o = -24$ V, $I_Z = 10$ mA

8. 4.35%, 1 Ω

9. V_o (min) = 11.31 V,
V_o (max) = 13.72 V,
P_D (max) = 7.566 W

10. 0.691 W, 1.62 W

11. −7.5 V, 2.25 W

12. (a) 1.25 V, (b) 13.75 V,
(c) 1.25 V, (d) 1.25 V

CHAPTER 15

Switched Mode Power Supplies

Learning Objectives

After completing this chapter, you will learn the following:

- Difference between a linearly regulated and switched mode power supply.
- Types of switched mode power supplies.
- Operational basics and design of flyback-type DC-to-DC converter.
- Operational basics of forward converter.
- Operational basics and design of push–pull converters.
- Types of switching regulators: Buck regulators, boost regulators, inverting regulators and three-terminal switching regulators.
- Connecting power converters in series and parallel.

Power supplies are often classified as linear power supplies or switched mode power supplies depending upon the nature of regulation circuit. Linear power supplies were discussed in Chapter 14. The focus in this chapter is on switched mode power supplies. In the case of switched mode power supplies, the unregulated DC input voltage is chopped at a high frequency with the help of an active device such as bipolar junction transistor, power MOSFET or insulated gate bipolar transistor (IGBT) and a transformer. The chopped waveform is then rectified and filtered to get the desired DC voltage. A sample of output voltage is used as a feedback signal to control some parameter of the drive waveform such as the duty cycle of the active device to achieve regulation. Switched mode power supply concept is the contemporary power supply design option for almost every conceivable requirement due to host of advantages it brings along with, which include high conversion efficiency, small size and weight and capability to generate any desired DC voltage from any available DC input. This chapter covers at length operational basics, design guidelines and role of integrated circuits in switched mode power supply design and other relevant topics. The text is supplemented by a large number of solved examples.

15.1 Switched Mode Power Supplies

As outlined earlier, based on the regulation concept, power supplies are classified as either linear or switched mode power supplies. Conventional AC/DC power supplies comprising a transformer, rectifier, filter and regulator (series or shunt type) constitute the linear power supply. The active device in the regulator circuit is always operated in the active or linear region of its output characteristics. Any change in the output voltage due to change in the input voltage or load current results in change in the voltage drop

across the regulator transistor (in the case of a series regulator) or a change in the current through the regulator transistor (in the case of a shunt regulator) so as to maintain a constant output voltage across the load. Linearly regulated power supplies were discussed in Chapter 14.

DC-to-DC converters and DC-to-AC inverters belong to the category of switched mode power supplies (SMPS). Besides there are switching supplies operating from mains called off-line switching supplies. An off-line switching supply can be distinguished from a conventional AC–DC supply as in the case of the former the AC mains is rectified and filtered without using an input transformer, and the DC voltage so obtained is then used as an input to a switching type DC-to-DC converter.

In a SMPS, the active device that provides regulation is always operated in a switched mode, that is, it is operated either in cut-off or in saturation. The input DC is chopped at a high frequency (typically 10 kHz to 100 kHz) using an active device [bipolar junction transistor (BJT), metal oxide semiconductor field effect transistor (MOSFET), insulated gate bipolar transistor (IGBT) or silicon-controlled rectifier (SCR)] and the converter transformer. The transformed chopped waveform is rectified and filtered. A sample of the output voltage is used as feedback signal for the drive circuit for the switching transistor to achieve regulation.

Linear versus Switched Mode Power Supplies

Some of the salient features of linear and switched mode power supplies are presented in the following paragraphs for the purpose of comparison between the two:

1. Linear power supplies are well known for their extremely good line and load regulation, low output voltage ripple and almost negligible radio frequency interference (RFI)/electro magnetic interference (EMI).
2. Switching power supplies, on the other hand, have much higher efficiency (typically 80–90% against 50–60% in the case of linear supplies) and reduced size/weight for a given power-delivering capability.
3. Quite often, compactness and efficiency are two major selection criteria. An improved efficiency and reduced size/weight are particularly significant when designing a power supply for a portable system where there is a requirement of a number of different regulated output voltages.
4. Also, unlike linear supplies, efficiency in switching supplies does not suffer as the unregulated input to regulated output differential becomes large.
5. In portable systems operating from battery packs and requiring higher DC voltages for their operation, the switching supply is the only option. We cannot use a linear regulator to change a given unregulated input voltage to a higher regulated output voltage.

Different Types of SMPS

SMPS are designed in a variety of circuit configurations depending upon the intended application. Almost all switching supplies belong to one of the following three broad categories:

1. Flyback converters.
2. Forward converters.
3. Push–pull converters.

There are variations in the circuit configuration within each one of these categories of SMPS. For instance, in the category of flyback converters, we have *self-oscillating flyback converters* and the *externally driven flyback converters*. Again, in the externally driven flyback converters, there are isolation and non-isolation type configurations. Also, there are *DC-to-DC* and *off-line flyback converters*.

Similarly, there are different circuit configurations in the other two categories of switching supplies also. Although these configurations differ to an extent, the basic operational principle and the design criteria for different types belonging to one category remain more or less the same.

15.2 Flyback Converters

The self-oscillating flyback DC-to-DC converter is the most basic converter based on the flyback principle. The other type is the externally driven flyback DC-to-DC converter. The two types are described in the following sections.

Self-Oscillating Flyback DC-to-DC Converter

Figure 15.1 shows the circuit arrangement in a self-oscillating or ringing-choke flyback DC-to-DC converter. A switching transistor, a converter transformer, a fast recovery rectifier and an output filter capacitor make up a complete DC-to-DC converter. It is a constant output power converter as is evident from the operational principle of this type of configuration.

During the conduction time of the switching transistor, the current through the transformer primary starts ramping up linearly with a slope equal to V_{in}/L_P. Here L_P is the primary inductance. The voltages induced in the secondary and the feedback windings, respectively, make the fast recovery rectifier reverse-biased and hold the conducting transistor in the "ON"-state.

When the primary current reaches a peak value I_P, where the core begins to saturate, the current tends to rise very sharply. This sharp rise in current cannot be supported by the fixed base drive provided by the feedback winding. As a result, the switching transistor begins to come out of saturation.

This is a regenerative process that ends up in the transistor getting switched off. The magnetic field due to the current flowing in the primary winding collapses, thus reversing the polarities of the induced voltages. The fast recovery rectifier is forward-biased and the stored energy is transferred to the capacitor and the load through the secondary winding. Thus, energy is stored during the ON-time and transferred during the OFF-time.

Figure 15.2 shows the relevant waveforms, which include the waveforms for collector–emitter voltage (V_{ce}), emitter–base voltage (V_{be}), magnetic flux (ϕ) in the transformer core, primary current (I_p) and secondary current (I_s). The waveforms are self-explanatory. The collector–emitter voltage is initially equal to V_{in}. In the subsequent cycles, the collector–emitter voltage (V_{ce}) during the OFF-time equals $V_{in} + V_o/n$, where n is the transformer step-up ratio. Magnetic flux in the core rises from 0 to ϕ_{max} during the conduction period when the primary current rises from zero to its peak value. The flux decreases from ϕ_{max} to 0 during the OFF-time.

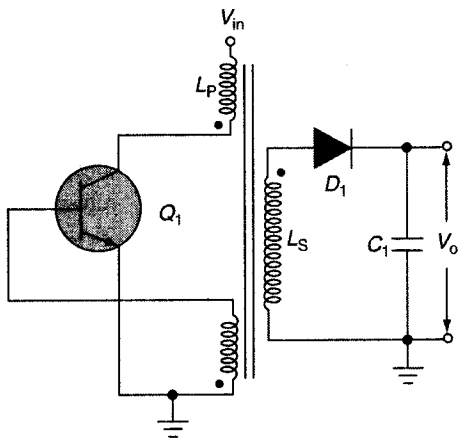


Figure 15.1 | Self-oscillating flyback DC-to-DC converter.

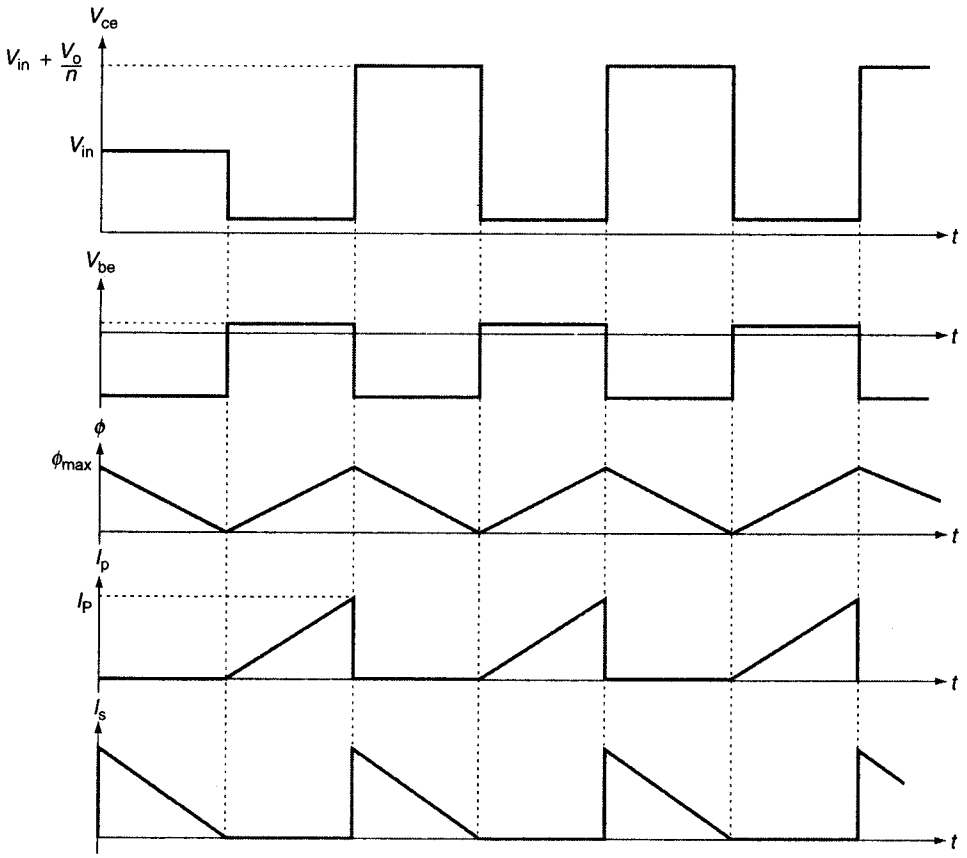


Figure 15.2 | Relevant waveforms in the case of self-oscillating flyback DC-to-DC converter.

The output capacitor supplies the load current during the ON-time of the transistor when no energy is being transferred from the primary side. It is a constant output power converter and the power that the converter can deliver to the load is equal to $(1/2) \times L_p \times I_p^2 \times f \times \eta$, which is the product of energy stored in the primary of the converter transformer $[(1/2) \times L_p \times I_p^2]$, switching frequency ($f$) and conversion efficiency (η). L_p and I_p are, respectively, the primary inductance and peak value of primary current. The output voltage reduces as the load increases and vice versa. Utmost care should be taken to ensure that the load is not accidentally taken off the converter. In that case, the output voltage would rise without limit until any of the converter components gets damaged. These converters are suitable for low output power applications due to their inherent nature of operation and may be used with advantage up to an output power of 150 W. They are characterized by high output voltage ripple.

Externally Driven Flyback DC-to-DC Converter

A variation of the self-oscillating flyback DC-to-DC converter is the externally driven flyback DC-to-DC converter (Figure 15.3). The basic principle remains the same. Energy is stored during turn-ON time and transferred during turn-OFF time of the active device. The feedback loop consisting of a comparator and the resistance divider provides the voltage sense as well as some degree of regulation.

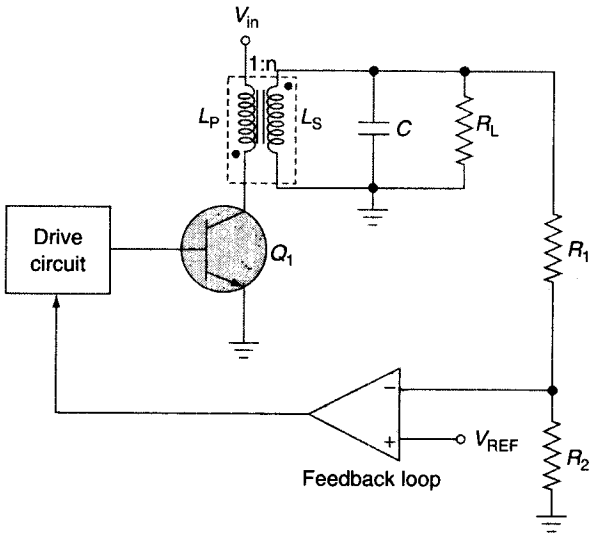


Figure 15.3 | Basic externally driven flyback DC-to-DC converter.

Extension of the converter circuit of Figure 15.3 is the externally driven flyback converter with pulse width modulation (PWM) control to achieve regulation. PWM is the most widely used control technique in conjunction with flyback converters. Figure 15.4 shows the circuit schematic. As the load current increases, the output voltage tends to fall. The PWM control senses the change and increases the turn-ON time so as to increase the power-delivering capability (increased turn-ON time means increased stored energy) and restores the output voltage. Similarly, an increase in the output voltage causes a reduction in the ON-time.

There are other control circuitries that provide regulation by changing the OFF-time rather than the ON-time. A reduced OFF-time increases the drive frequency and hence the power-delivering capability and vice versa.

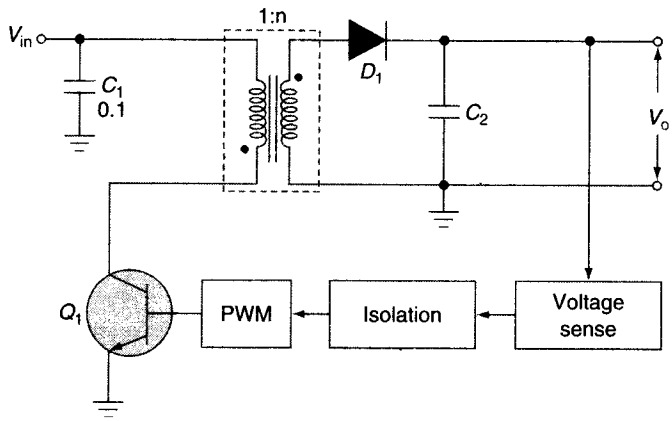


Figure 15.4 | Externally driven flyback DC-to-DC converter with PWM control.

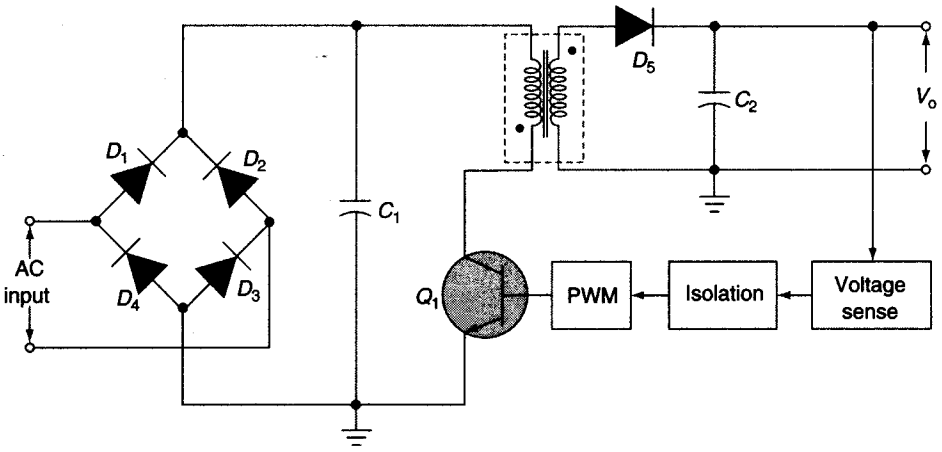


Figure 15.5 | Off-line externally driven flyback AC-to-DC converter.

A number of integrated circuits have been developed to provide drive and control functions for DC-to-DC converters. Some of these ICs provide PWM control while others offer constant ON-time and variable frequency operations. These ICs have built-in features like over-voltage protection, current limit and so on. Such ICs (TL497, TL494, TL594 and SG3524 to name a few) have considerably simplified the drive and control circuit design.

Most switching supplies used in consumer and industrial systems are off-line. Figure 15.5 shows an off-line externally driven flyback AC-to-DC converter. It is called off-line because the input voltage to the transistor switch is developed right from the AC line without first going through 50/60 Hz transformer. Bridge rectifier and the filter capacitor accomplish this in the circuit of Figure 15.5. The feedback loop in an off-line supply must have isolation so that the DC output is isolated from the AC line. A small transformer

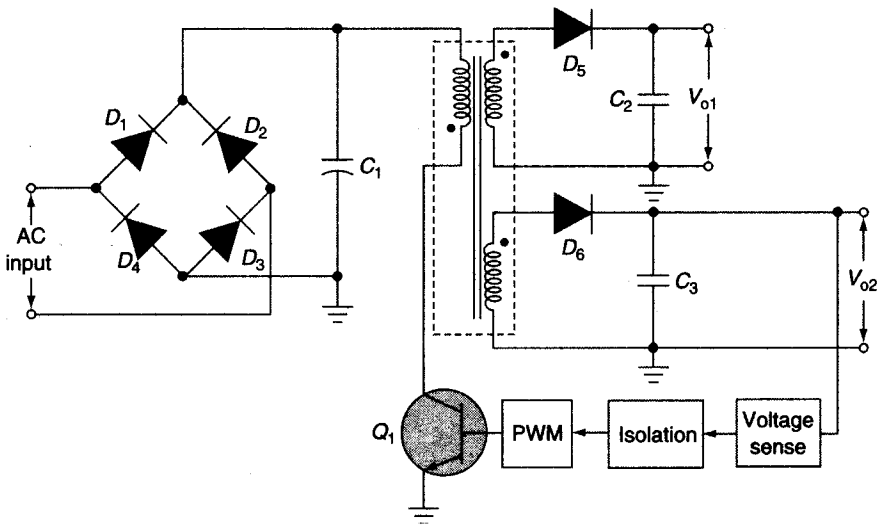


Figure 15.6 | Off-line flyback AC-to-DC converter with multiple outputs.

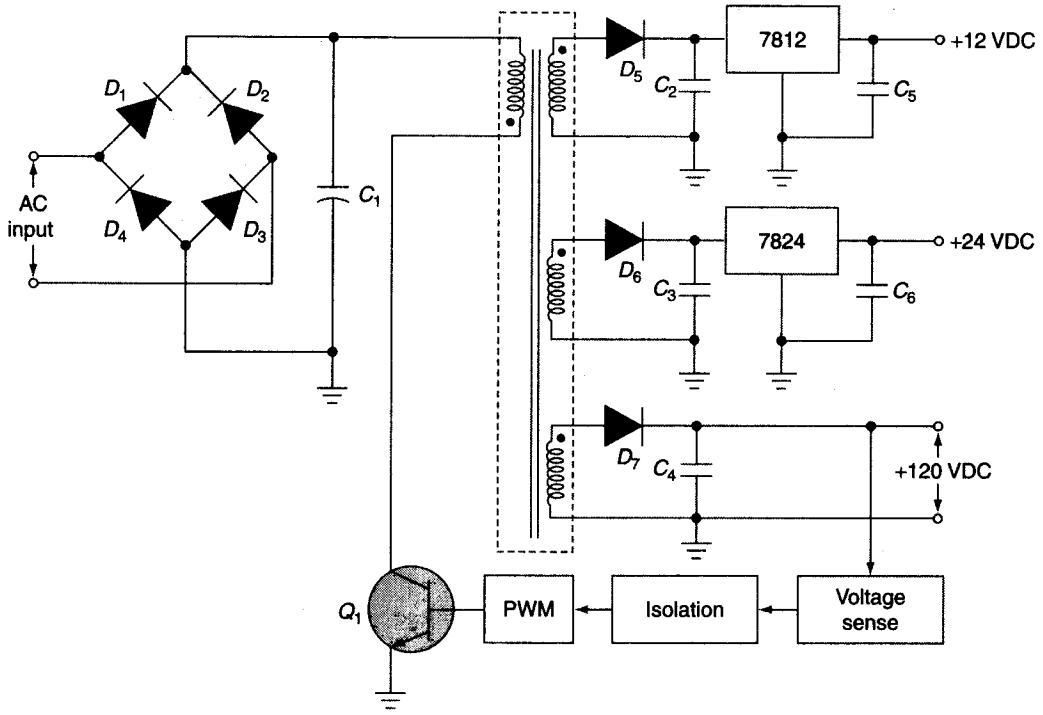


Figure 15.7 | Multi-output switching supply with post regulation.

or an opto-isolator usually accomplishes this. Most switching supplies are required to produce more than one regulated DC voltage. Figure 15.6 shows an off-line multiple output flyback DC-to-DC converter.

In case a more stringent regulation is required in respect of one or more outputs, linear post regulator can be used for the purpose as shown in Figure 15.7. Three-terminal IC regulators have been used here for the purpose.

Discontinuous and Continuous Operational Modes

There are two distinctly different operational modes of flyback converters. These are *discontinuous* mode and *continuous* mode. The circuit topology in the two cases is the same and it is the transformer's magnetizing inductance and the load current, which together decide the operational mode.

Figure 15.8 shows the primary and secondary current waveforms in the case of discontinuous mode of operation. The primary current starts from zero and ramps up to a peak value depending upon the magnetizing inductance, input DC voltage and turn-ON time of the switching device. As is evident from the waveforms, the energy stored during the turn-ON time of the switching device is completely transferred within the turn-OFF time. Increase in peak value of primary current due to increased turn-ON time necessitated by increased load current requirement produces an increased peak value of secondary current as shown by dotted lines. Consequently, the energy transfer time also increases. With further increase in load current requirement, a stage comes where the required energy transfer time equals the available turn-OFF time.

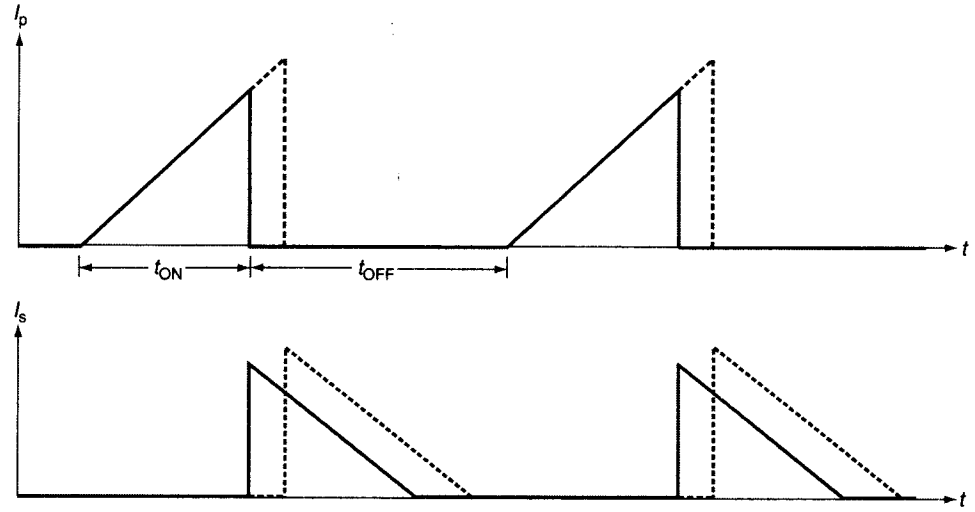


Figure 15.8 | Primary and secondary current waveforms for discontinuous mode of operation.

A still further increase in load current requirement would lead to incomplete energy transfer during the available turn-OFF time. This leads to the primary current in the next storage cycle to start from a DC value. The resulting primary and secondary current waveforms look like those shown in Figure 15.9. The converter in such a case is said to operate in continuous mode. It may be mentioned here that in the case of continuous mode of operation, increase in load current requirement initially causes an increase in peak value of primary current, and thus the area of primary current trapezoid, and a decrease in the area of the secondary current trapezoid as shown; after a few switching cycles, the circuit finally relaxes to a state where volt-seconds across primary during turn-ON and turn-OFF periods are equal.

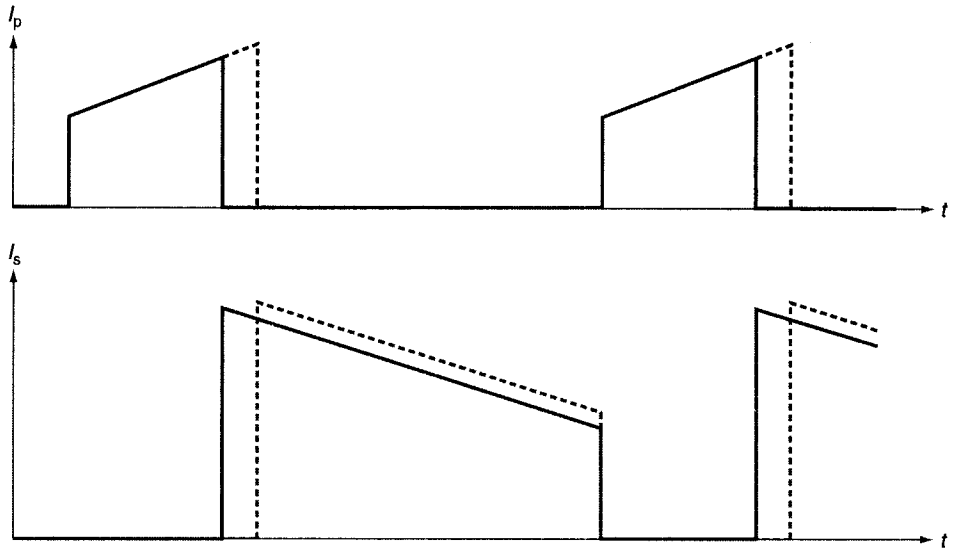


Figure 15.9 | Primary and secondary current waveforms for continuous mode of operation.

The discontinuous mode is characterized by relatively much higher peak values of primary and secondary currents and a consequent lower magnetizing inductance as compared to continuous mode. Owing to lower magnetizing inductance, it responds more rapidly and with a lower transient output voltage spike to sudden changes in load current requirement. Without going into details, which would be beyond the scope of this text, in the case of continuous mode of operation, the feedback error amplifier bandwidth needs to be drastically reduced to have stable operation. Owing of these reasons, discontinuous mode is more widely used than the continuous mode despite the fact that the former has more severe radio frequency interference (RFI) problems. In the following section the basic design procedure for an externally driven flyback DC-to-DC converter operating in the discontinuous mode is discussed.

Design Procedure for Externally Driven Flyback DC-to-DC Converter

Design procedure for self-oscillating type and externally driven flyback DC-to-DC converters is the same except that in the case of the former, the switching transformer also has a feedback winding to generate the drive waveform for the switching transistor. In that case, one also needs to determine the number of turns for the feedback winding. Figure 15.10 shows the basic schematic arrangement of an externally driven flyback converter. Let

V_{in} = Input voltage in volts
V_o = Output voltage in volts
P_o = Output power to be delivered to load in watts
P_{in} = Power drawn from input source of power in watts
η = Expected conversion efficiency
t_{ON} = Conduction time in seconds
L_P = Primary inductance in Henries
I_P = Peak primary current in Amperes
I_S = Peak secondary current in Amperes
N_P = Primary turns
N_S = Secondary turns
B_{max} = Maximum flux density in the core in Tesla
ϕ = Magnetic flux in the core in Weber
A_C = Core cross-section in cm^2
W_A = Window area in cm^2
f = Switching frequency in Hz

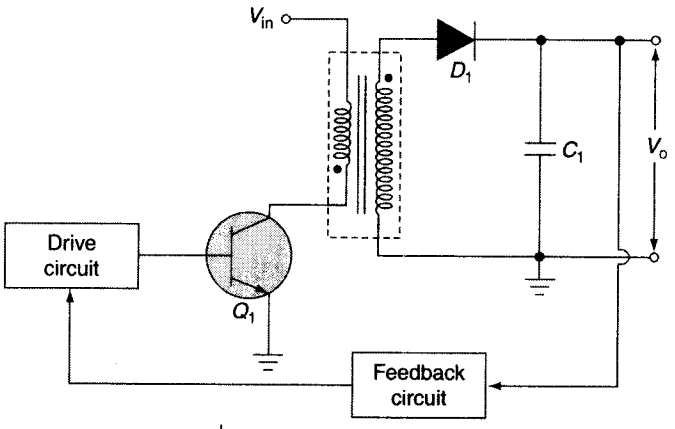


Figure 15.10 | Externally driven flyback converter.

The key component of the design exercise is the design of switching transformer. In the following paragraphs is presented step-by-step procedure for design of switching transformer for a flyback DC-to-DC converter.

The first step is to determine the size of the core in terms of the minimum area product required to deliver the desired amount of power to the load for the chosen values of operating frequency and maximum allowable temperature rise of the core. The area product is the product of winding window area and the cross-sectional area of the core. Manufacturers of transformer cores often provide nomograms indicating the power-handling capability of different types of cores manufactured by them as a function of operating frequency and given temperature rise. Designers can use these nomograms to choose suitable core for their application. These nomograms are, however, specific to the cores offered by the manufacturer. One such representative family of curves for toroidal ferrite cores is shown in Figure 15.11. Equation (15.1) gives a generalized expression to compute the required area product from known values of input power, operating frequency and maximum permissible flux density. Area product ($W_A A_C$) in cm^4 is given by

$$W_A A_C = \left[\frac{11 \times P_{in}}{K \times f \times B_{max}} \right]^{1.143} \tag{15.1}$$

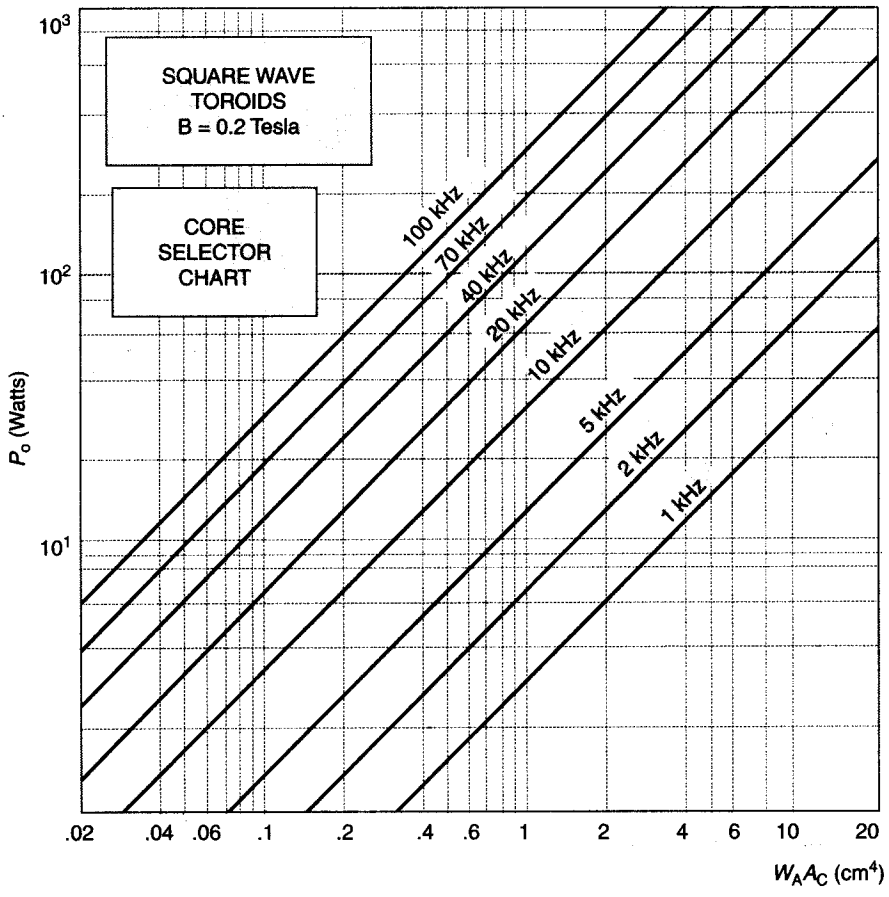


Figure 15.11 | Power versus area product ($W_A A_C$) as function of switching frequency.

P_{in}, f and B_{max} are substituted, respectively, in W, Hz and T; K is the overall copper utilization factor and is the product of three factors, namely, primary area factor (ratio of effective primary area to the available window winding area), winding packing factor (typically 0.35–0.4) and RMS current factor (ratio of effective DC input current to RMS value of primary current). K is typically in the range of 0.1 to 0.2.

When the switching transistor is switched on for a time period equal to t_{ON}, then the peak primary current I_P can be computed from

$$V_{in} = \frac{L_P \times I_P}{t_{ON}} \tag{15.2}$$

$$V_{in} \times t_{ON} = L_P \times I_P$$

Also,

$$P_{in} = \frac{P_o}{\eta} \quad \text{and} \quad P_{in} = \frac{L_P \times I_P^2 \times f}{2}$$

therefore

$$2P_o = \eta \times L_P \times I_P^2 \times f \tag{15.3}$$

Equations (15.2) and (15.3) can be solved simultaneously to get L_P and I_P as

$$I_P = \frac{2P_o}{V_{in} \times t_{ON} \times \eta \times f} \tag{15.4}$$

$$L_P = \frac{V_{in}^2 \times t_{ON}^2 \times \eta \times f}{2P_o} \tag{15.5}$$

The next step is to determine the number of primary turns that would not saturate the core. From first principles,

$$V_{in} = N_P \times \frac{d\phi}{dt}$$

$$= \frac{N_P \times B_{max} \times A_e}{t_{ON}}$$

$$N_P = \frac{V_{in} \times t_{ON}}{B_{max} \times A_e} \tag{15.6}$$

where A_e is the effective area of core cross-section. B_{max} to be substituted in the above expression should be a little less than the B_{max} rating of the chosen core material. Having determined primary turns, the next step is to determine the size of air gap that would give a primary inductance of L_P with N_P number of primary turns. Primary inductance can also be computed from

$$L_P = \frac{\mu_o \times \mu_r \times N_P^2 \times A_e}{l_e} \tag{15.7}$$

where μ_o is the permeability of free space = $4\pi \times 10^{-7}$ H/m; μ_r the initial relative permeability of the chosen core material; l_e the effective magnetic path length. Equation (15.7) is first used to determine the value of effective permeability μ_e that would make N_P turns of the primary winding give L_P Henries of primary inductance. Having determined the value of μ_e, the size of the air gap can then be found from

$$l_g = \frac{l_e}{\mu_e} \tag{15.8}$$

As the third step, the number of secondary turns can be determined from the known value of primary turns and the step-up ratio n. The step-up ratio is primarily decided by the $V_{CEO(max)}$ rating of the bipolar transistor or the $V_{DS(max)}$ rating of the MOSFET depending upon the switching device used in the circuit. In the case of bipolar transistor switch, during the turn-OFF time of the device, maximum voltage that appears across the collector–emitter terminals is given by $V_{in} + V_o/n$, where $n = N_S/N_P$. Therefore

$$V_{CEO(max)} = V_{in} + \frac{V_o}{n}$$

$$n = \frac{V_o}{V_{CEO(max)} - V_{in}}$$

This gives

$$N_S = \frac{N_P \times V_o}{V_{CEO(max)} - V_{in}} \tag{15.9}$$

Again, $V_{CEO(max)}$ to be substituted in Eq. (15.9) should be less than the $V_{CEO(max)}$ rating given in the transistor's data sheet. Drive circuit parameters can be determined from the required value of the base current I_B:

$$I_B = \frac{I_P}{h_{FE(min)}} \tag{15.10}$$

Primary and secondary wire sizes can be determined from calculated RMS values of primary and secondary currents.

Diode D_1 in Figure 15.10 should be a fast recovery rectifier. A fast recovery rectifier ensures that it is fully reverse-biased and there is no leakage of power during the conduction time of the transistor. The peak inverse voltage (PIV) rating of the rectifier should be more than twice the desired output voltage.

Capacitor C_1 should be such that time constant C_1R_L provides the desired output ripple specification. C_1R_L should be much larger than the turn-ON time of the switching device. It is chosen to be at least 10 times the turn-ON time (t_{ON}). That is

$$C_1 \times R_L = 10 \times t_{ON}$$

$$C_1 \times \left(\frac{V_o^2}{P_o}\right) = 10 \times t_{ON}$$

This gives

$$C_1 = \frac{10 \times t_{ON} \times P_o}{V_o^2} \tag{15.11}$$

In the case of self-oscillating flyback converter, one would also need to determine the number of turns N_B in the feedback winding. This is done on the basis of producing a voltage equal to $2V_{BE}$ across the base or feedback winding during the conduction time of the transistor. Out of $2V_{BE}$ voltage, V_{BE} is dropped across the resistance usually connected in series with base terminal and the remaining V_{BE} appears across the emitter–base junction. That is

$$N_B = N_P \times \left(\frac{2 \times V_{BE}}{V_{in}}\right) \tag{15.12}$$

EXAMPLE 15.1

Figure 15.12 shows the basic ringing-choke flyback DC-to-DC converter along with the drive waveform across the feedback winding and the primary current waveform. From the data given in the circuit diagram, determine output voltage across the load resistance R_L if the conversion efficiency were 80%.

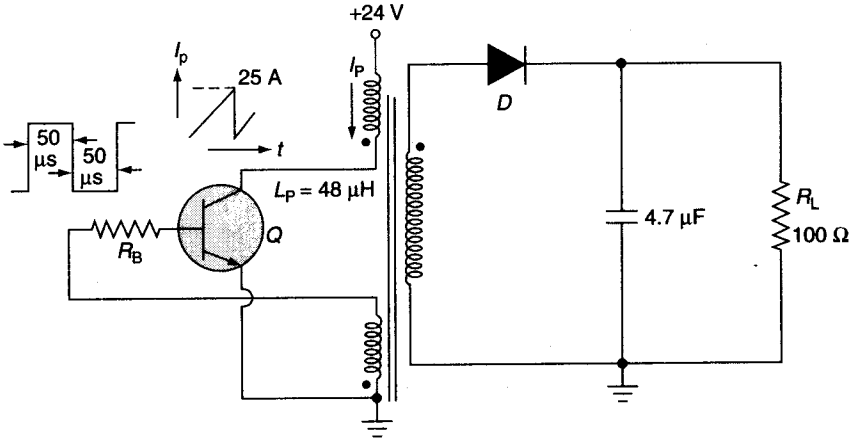


Figure 15.12 | Example 15.1.

Solution

1. Power delivered by the converter of this type is given by the product of power stored in the primary of the switching transformer and the conversion efficiency. That is, power delivered = power stored × conversion efficiency.
2. Power stored in turn is equal to the product of energy stored and the switching frequency. That is, power stored = $(1/2)L_P I_P^2 f$.
3. $f = 1/(50 \times 10^{-6} + 50 \times 10^{-6})$ Hz = 10 kHz.
4. Therefore, power stored = $(1/2) \times 48 \times 10^{-6} \times 25 \times 25 \times 10 \times 10^3 = 150$ W.
5. Power delivered to load resistance $R_L = 150 \times 0.8 = 120$ W.
6. If V_o were the voltage across R_L, then

   $V_o^2/R_L = 120$, which gives $V_o = \sqrt{120 R_L} = \sqrt{120 \times 100} = 109.55$ W

Answer: Voltage across load resistance, $R_L = 109.55$ W.

EXAMPLE 15.2

A flyback DC-to-DC converter operating in discontinuous mode is to deliver a power of 50 W to a load resistance of 5000 Ω. The converter operates from a regulated input of 24 VDC and produces 500 V across the load resistance. The toroidal core chosen for the purpose is capable of delivering the desired output power at a switching frequency of 20 kHz and flux density of 3000 gauss and has the following dimensional parameters.

(a) Effective magnetic path length, $l_e = 6.2$ cm

(b) Effective cross-sectional area, $A_e = 0.4$ cm^2

Design the switching transformer assuming a conversion efficiency of 80% and the $V_{CEO(max)}$ rating of the switching transistor as 100 V.

Solution

1. $f = 20$ kHz. For a symmetrical drive waveform,
$$t_{ON} = t_{OFF} = 1/(2 \times 20 \times 10^3)\ \text{s} = 25\ \mu\text{s}$$
2. As a first step, we will find the required values of primary inductance and the corresponding peak primary current. These can be determined from Eqs. (15.4) and (15.5) as follows:
$I_P = 2P_o/V_{in}t_{ON}\eta f$ and $L_P = V_{in}^2 t_{ON}^2 \eta f/2P_o$
$I_P = (2 \times 50)/(24 \times 25 \times 10^{-6} \times 0.8 \times 20 \times 10^3) = 100/9.6 = 10.4$ A
$L_P = (24 \times 24 \times 25 \times 10^{-6} \times 25 \times 10^{-6} \times 0.8 \times 20 \times 10^3)/(2 \times 50) = 57.6\ \mu\text{H}$
3. Number of primary turns can be determined from Eq. (15.6) as follows:
$$N_P = V_{in}t_{ON}/B_{max}A_e$$
$$= (24 \times 25 \times 10^{-6})/(0.3 \times 0.4 \times 10^{-4}) = 50$$
5. Equation (15.7) can be used to determine the value of permeability required for 50 turns of primary winding to produce a primary inductance of 57.6 μH as follows:
$L_P = \mu_0\mu_r N_P^2 A_e/l_e$
$\mu_r = L_P l_e/\mu_0 N_P^2 A_e$
$= (57.6 \times 10^{-6} \times 6.2 \times 10^{-2})/(4 \times 3.14 \times 10^{-7} \times 50 \times 50 \times 0.4 \times 10^{-4})$
$= (357.12 \times 10^{-8})/(1.256 \times 10^{-7}) = 28.43$
6. Size of the air gap can be computed from Eq. (15.8) as follows:
$$l_g = 6.2/28.43\ \text{cm} = 2.2\ \text{mm}$$
7. Assuming permissible collector-to-emitter voltage at turn-OFF equal to 75% of the $V_{CEO(max)}$ rating of the switching transistor, the step-up ratio (n) can be computed as follows:
$$n = V_o/(V_{CEO(max)} - V_{in}) = 500/(75 - 24) = 500/51 = 9.8$$
Therefore, number of secondary turns, $N_S = 50 \times 9.8 = 490$.
8. Primary and secondary wire sizes can be determined from calculated RMS values of primary and secondary currents, respectively.

Answer: Primary inductance $L_P = 57.6$ μH, number of primary turns = 50, permeability $\mu_r = 28.43$, size of the air gap = 2.2 mm, step-up ratio (n) = 9.8, number of secondary turns $N_S = 490$.

15.3 Forward Converter

Forward converter is another popular SMPS configuration. Figure 15.13 shows the basic circuit diagram of an off-line forward converter. There are some fundamental differences between a flyback converter and a forward converter. In the case of circuit diagram shown in Figure 15.13, when the transistor switch is turned ON, the polarities of the transformer windings (as indicated by the position of dots) are such that diode D_5 is forward-biased and diodes D_6 and D_7 are reverse-biased. Most of the energy in a forward converter is stored in the output inductor rather than the transformer primary used to store energy in a flyback converter. When the transistor switch is turned OFF, the magnetic field collapses. Diode D_5 is reverse-biased and diodes D_6 and D_7 are forward-biased. As the current through an inductance cannot

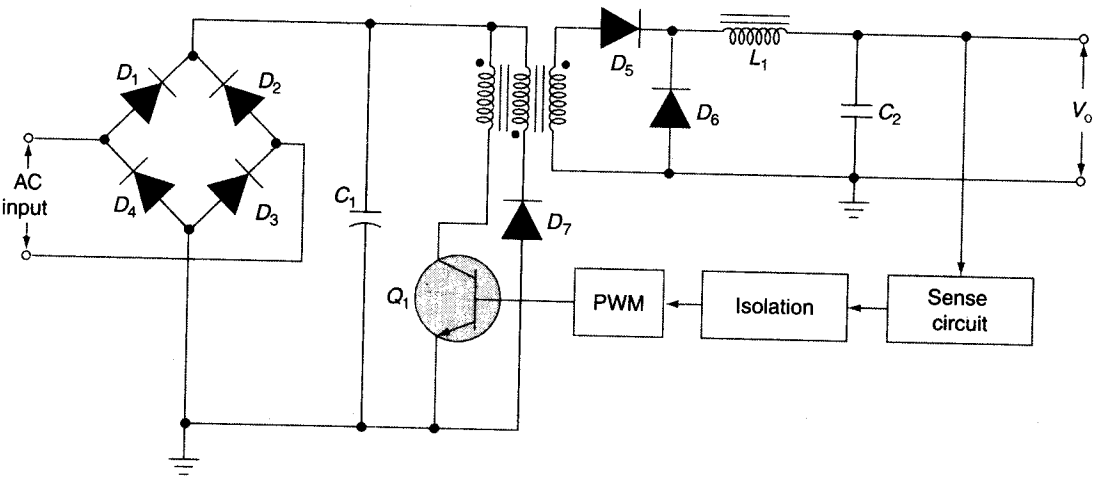


Figure 15.13 | Basic off-line forward converter.

change instantaneously, the output current continues to flow through the output and the forward-biased diode D_6 provides the current path.

Unlike a flyback converter, current in a forward converter flows from the energy storage element during both halves of the switching cycle. Thus for the same output power, a forward converter has much less output ripple than a flyback converter. Controlling the duty cycle of the transistor switch provides output regulation.

In the absence of the third winding and diode D_7, a good fraction of energy stored in the transformer primary is lost. This effect is more severe at higher switching frequencies. The third winding and the forward-biased diode D_7 return the energy, which would otherwise be lost and reset the transformer core after each operating cycle. This not only increases converter efficiency but also makes the converter transformer core immune to saturation problems.

15.4 Push–Pull Converter

Push–pull converter is the most widely used SMPS configuration belonging to the family of forward converters. There are several different circuit configurations within the push–pull converter sub-family. These circuits differ only in the mode in which the transformer primary is driven. These include the conventional two-transistor, one-transformer push–pull converter (both self-oscillating and extremely driven type); two-transistor, two-transformer push–pull converter; half-bridge converter and full-bridge converter.

Figure 15.14 shows the conventional self-oscillating two-transistor, one-transformer push–pull converter. Base resistors R_{B1} and R_{B2} are equal in magnitude. Its operation can be explained by considering it equivalent to two alternately operating self-oscillating flyback converters. When transistor Q_1 is in saturation, energy is stored in the upper half of the primary winding. When the linearly rising current reaches a value where the transformer core begins to saturate, the current tends to rise sharply, which is not supported by a more or less fixed base bias. The transistor Q_1 starts to come out of saturation. This is a regenerative process and ends up in switching off transistor Q_1 and switching on transistor Q_2. Thus transistors Q_1 and Q_2 switch ON and OFF alternately. When Q_1 is ON, energy is being stored in the upper half of the primary and the energy stored in the immediately preceding half cycle in the lower half of the primary winding (when transistor Q_2 was ON) is getting transferred. Thus energy is stored and transferred at the

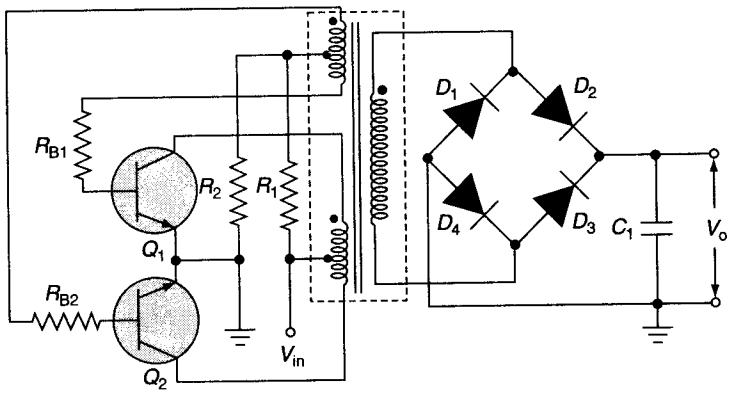


Figure 15.14 | Basic self-oscillating push–pull converter.

same time. The voltage across secondary is a symmetrical square waveform, which is then rectified and filtered to get the DC output.

As the primary is center-tapped, and only half of the primary winding is active at a time, the transformer is not utilized as well as it is in the case of other forms of push–pull converter, like half-bridge and full-bridge converters. Also, in this type of converter, switching transistors operate at collector stress voltages of at least twice the DC input voltage. As a result, a push–pull converter is not a highly recommended choice for off-line operation. A push–pull converter that has wider applications than its self-oscillating counterpart is the extremely driven push–pull converter (Figure 15.15). This has been possible due to availability of a variety of SMPS drive and control ICs.

Self-oscillating push–pull converters are frequently used along with a voltage multiplier chain to design a high-voltage, low-current power supply (Figure 15.16). This configuration is particularly useful for designing helium–neon laser power supplies. The basic push–pull converter converts the low DC input voltage to a stepped-up square waveform, which is then multiplied using a chain of diodes and capacitors.

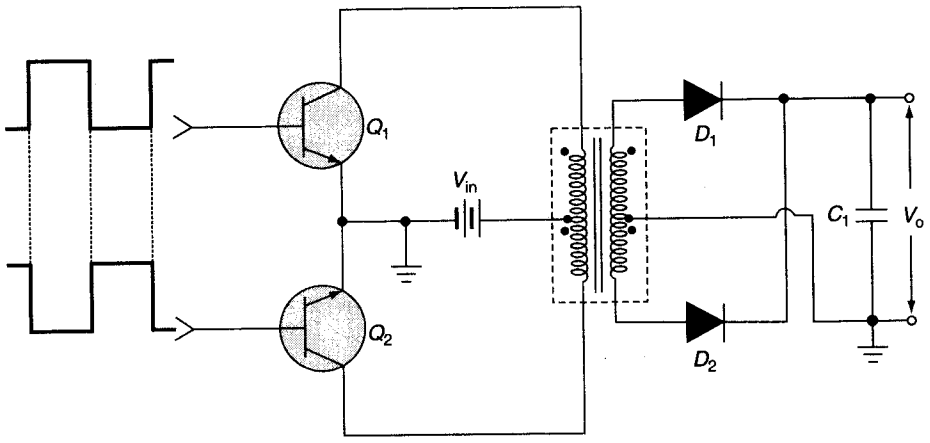


Figure 15.15 | Externally driven push–pull converter.

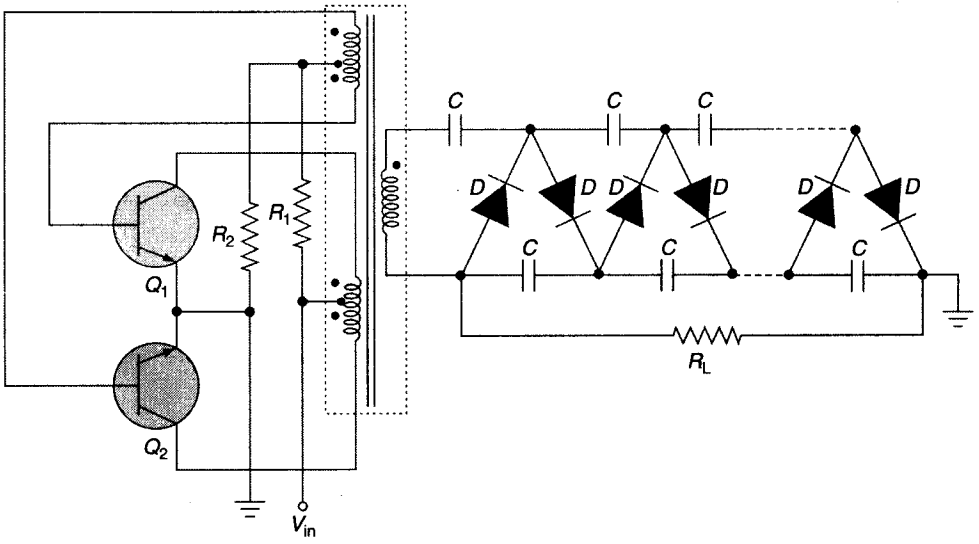
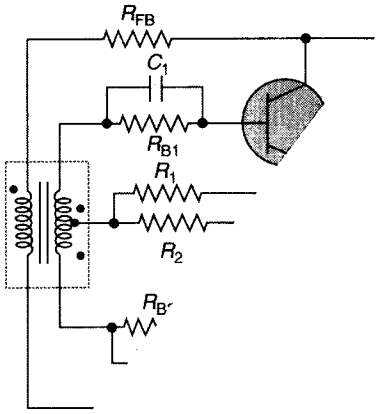


Figure 15.16 | Self-oscillating push–pull converter with voltage mu

In the self-oscillating two-transistor, one-transformer push–pull conve
both power transformation as well as power switching. This circuit has
power switching is done at output power levels, the converter efficien
high power converter. Second, the peak collector current depends up
gain and input characteristics and is dependent on load. As there
from device to device, the circuit performance depends upon t
former core must be the expensive square loop material with

These problems are overcome in the two-transformer, tw
Power switching is done at base power level and the o



only. Capacitors C_1 and C_2 are the speed-up capacitors (also known as commutating capacitors) used to achieve a faster turn-OFF of the respective transistors.

Half-bridge converter (Figure 15.18) is recommended for high power applications. Transistors Q_1 and Q_2 operate alternately. The half-bridge converter has the advantage that it allows the use of transistors with lower breakdown voltages.

The *full-bridge converter* (Figure 15.19) has the advantage that the highest voltage any transistor is subjected to is only V_{in} against $2V_{in}$ as in the case of self-oscillating push–pull converter. Owing to reduced voltage and stress on the transistors, full-bridge converter offers great reliability.

Design Procedure for Push–Pull DC-to-DC Converter

In the following paragraphs, we will outline procedure for designing the basic self-oscillating push–pull DC-to-DC converter employing two-transistor, single transformer circuit topology. Figure 15.20 shows

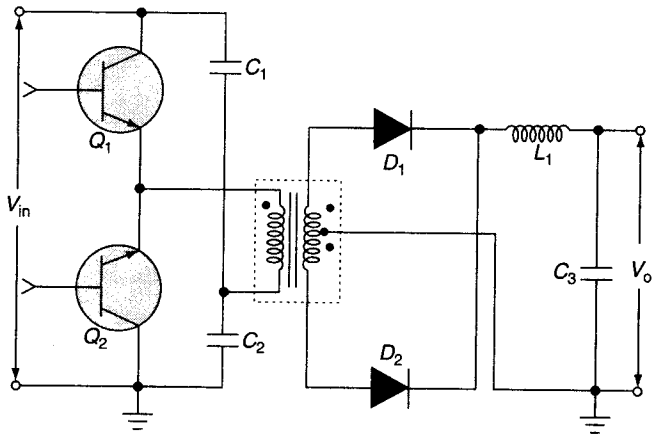


Figure 15.18 | Half-bridge converter.

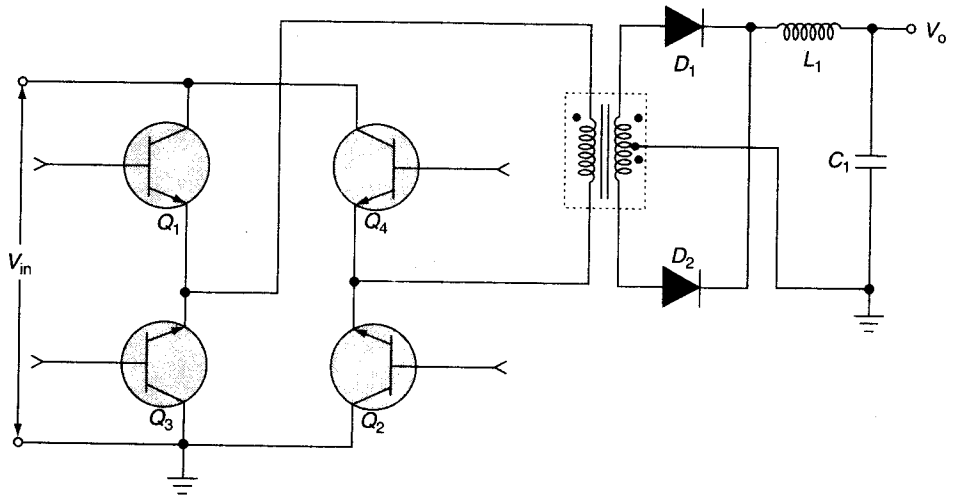


Figure 15.19 | Full-bridge converter.

the circuit diagram along with the relevant waveforms. The operational principle of this type of converter has already been described in the previous paragraphs. Step-by-step design procedure is outlined as follows.

The first step is to determine the size of the core in terms of the minimum area product required to deliver the desired amount of power to the load for the chosen values of operating frequency and maximum allowable temperature rise of the core. The selection of the core size is done either with the help of nomograms provided by the manufacturer or by using the generalized expression given by Eq. (15.1).
From the first principles,

$$V_{in} = N_P \times \frac{d\phi}{dt} \tag{15.13}$$

where N_P is the number of primary turns in the collector circuit of either of the two switching transistors and is equal to half of the primary turns.

It is evident from the waveforms that the magnetic flux varies from $-\phi_{max}$ to $+\phi_{max}$ or $+\phi_{max}$ to $-\phi_{max}$ when either of the two transistors is conducting. In both cases, change in magnetic flux equals $2\phi_{max}$. That is

$$d\phi = 2 \times \phi_{max}$$

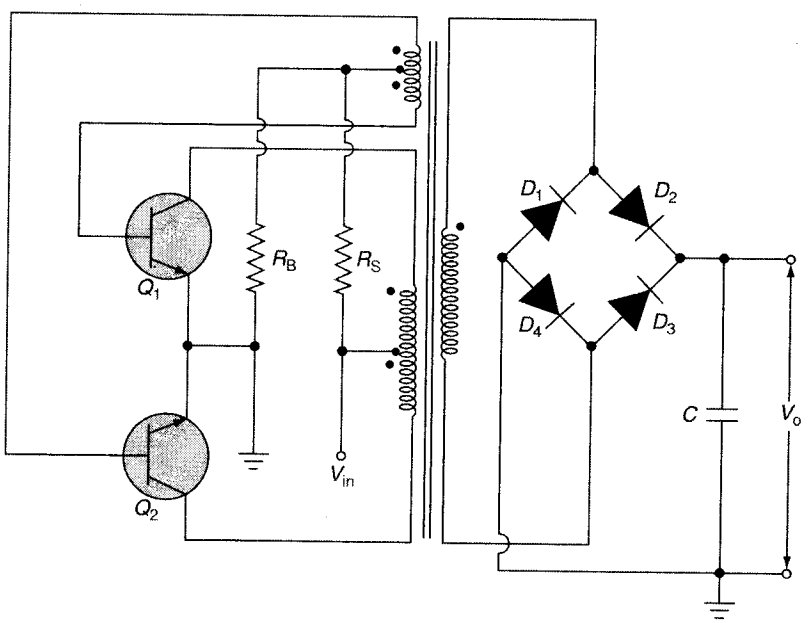
Also, this change in flux occurs in a time period equal to half of the total time period. That is

$$dt = 0.5 \times T$$

where T is the time period of switching waveform, that is, $T = 1/f$, f being the switching frequency. Therefore,

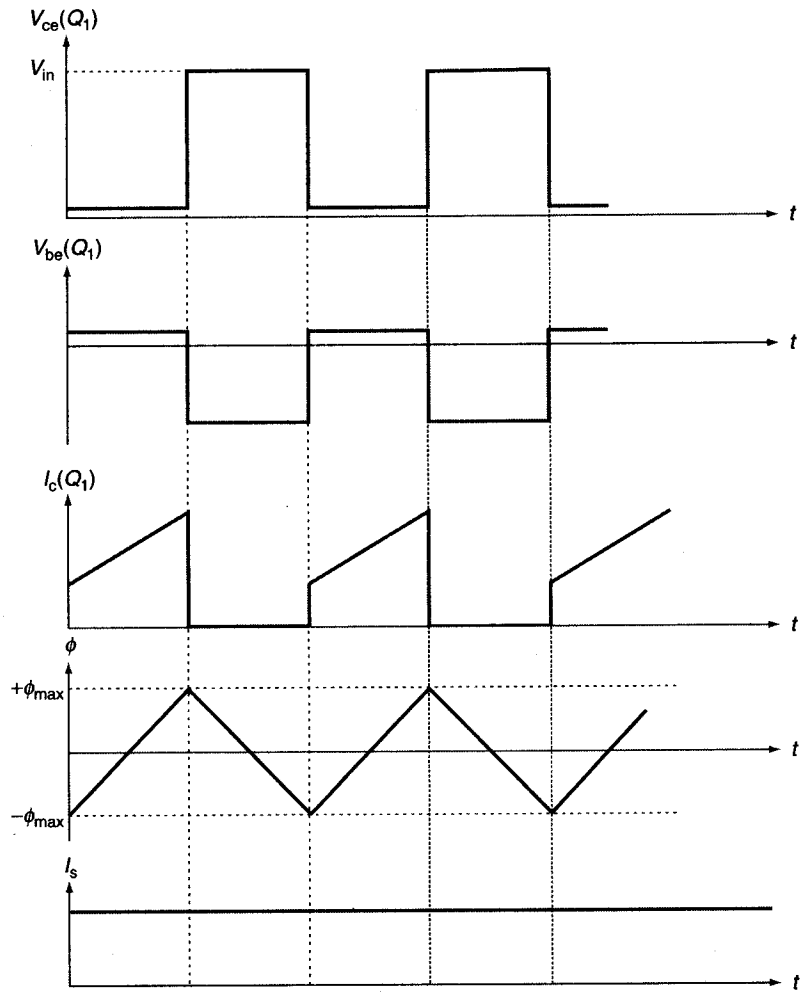
$$dt = 1/(2 \times f)$$

Substituting for $d\phi$ and dt in Eq. (15.13), we get



(a)

Figure 15.20 | Self-oscillating push–pull converter: (a) Circuit diagram; (b) waveforms.



(b)

Figure 15.20 | *Continued.*

$$V_{in} = N_P \times \frac{2 \times \phi_{max}}{1/(2 \times f)} = 4 \times N_P \times \phi_{max} \times f \tag{15.14}$$

Now

$$\phi_{max} = B_{max} \times A_e$$

where B_{max} is the maximum flux density in the core and A_e the effective area of core cross-section. This gives

$$V_{in} = 4 \times N_P \times B_{max} \times A_e \times f \tag{15.15}$$

Equation (15.15) can used to determine the number of primary turns:

$$N_p = \frac{V_{in}}{4 \times B_{max} \times A_e \times f} \tag{15.16}$$

Number of secondary turns N_S can be computed from the following equation:

$$N_S = N_P \times \left(\frac{V_o}{V_{in}} \right) \tag{15.17}$$

From the known values of primary turns and core parameters, primary inductance can be determined from

$$L_P = \frac{\mu_o \times \mu_r \times N_P^2 \times A_e}{l_e} \tag{15.18}$$

The primary inductance then determines the peak value of primary current, which can be computed as follows:

$$V_{in} = L_P \times \left(\frac{dI_P}{dt} \right) = \frac{2 \times L_P \times I_P}{0.5 \times T} = 4 \times L_P \times I_P \times f$$

Therefore,

$$I_P = \frac{V_{in}}{4 \times L_P \times f} \tag{15.19}$$

Maximum value of transistor's collector current is then given by

$$I_{C(max)} = I_P + I_{AV} = I_P + \frac{P_o}{\eta \times V_{in}} = \left(\frac{V_{in}}{4 \times L_P \times f} \right) + \left(\frac{P_o}{\eta \times V_{in}} \right) \tag{15.20}$$

The chosen transistors should be capable of handling collector current as given by Eq. (15.20). Maximum value of collector-to-emitter voltage appearing across each of the transistors equals $[2V_{in} + V_{BE}$ (winding)]. $V_{CEO(max)}$ of the chosen transistor should be about 25–30% higher than this value.

N_B can be determined in the same way as in the case of self-oscillating flyback converter. That is

$$N_B = N_P \times \left(\frac{2 \times V_{BE}}{V_{in}} \right) \tag{15.21}$$

R_B should be such that it produces a voltage of 0.6 V at the center tap of the feedback winding. That is

$$V_{in} \times \left(\frac{R_B}{R_B + R_S} \right) = 0.6$$

$$R_S = R_B \times \left[\frac{V_{in} - 0.6}{0.6} \right] \tag{15.22}$$

D_1–D_4 are rectifier diodes. These diodes should have the requisite peak inverse voltage (PIV) and forward current ratings. Again, capacitor C is chosen to meet the specified output ripple requirement. Capacitor C is usually chosen to make CR_L time constant much larger than (usually 100 times) the period T. That is

$$C \times R_L \geq 100 \times T$$

$$C \geq \frac{100}{R_L \times f}$$

Substituting $R_L = V_O^2 / P_O$ in the expression for C, we get

$$C \geq \left(\frac{100 \times P_o}{V_o^2 \times f} \right) \tag{15.23}$$

EXAMPLE 15.3

An externally driven push–pull DC-to-DC converter is to be designed to deliver a power of 100 W to a load resistance of 10 kΩ. The converter operates from a regulated input of 12 VDC and produces 1000 V across the load resistance. The toroidal core chosen for the purpose is capable of delivering the desired output power at a switching frequency of 20 kHz and flux density of 2000 gauss and has the following dimensional parameters.

(a) Effective magnetic path length, $l_e = 8.3$ cm
(b) Effective cross-sectional area, $A_e = 0.57$ cm^2

Assuming core permeability and conversion efficiency to be 3000 and 80% respectively, design the transformer by determining primary and secondary number of turns and the relevant currents that would enable choose the right wire gauge for the primary and secondary windings. Assume two-transistor, single transformer topology and a symmetrical drive waveform.

Solution

1. As a first step, we will determine the number of primary turns, N_p.

$$N_p = V_{in}/(4B_{max}A_e f)$$
$$= 12/(4 \times 0.2 \times 0.57 \times 10^{-4} \times 20 \times 10^3) = 13.16$$

2. Primary winding can be taken as 14–0–14 center-tapped winding.

3. Number of secondary turns,

$$N_S = N_P(V_o/V_{in})$$
$$N_S = 14 \times 1000/12 = 1167$$

4. The primary current in each half of the primary winding flows for half of the period of the switching waveform and is equal to the sum of magnetizing current and a DC component. It is given by Eq. (15.20).

Primary current $= (V_{in}/4L_p f) + (P_o/\eta V_{in})$

$L_p = \mu_0 \mu_r N_p^2 A_e/l_e$

$= 4 \times 3.14 \times 10^{-7} \times 3000 \times 14 \times 14 \times 0.57 \times 10^{-4}/8.3 \times 10^{-2} = 507\ \mu H$

5. Therefore maximum value of primary current for one-half of the period of switching waveform is given by

$[12/(4 \times 507 \times 10^{-6} \times 20 \times 10^3)] + [100/(0.8 \times 12)] = 0.3 + 10.4 = 10.7$ A

6. RMS value of primary current can be determined from the maximum value of the current and the wave shape. In the present case, the waveform is almost a square waveform with a flat top and a duty cycle of 0.5 as the DC component is much larger than the magnetizing component. RMS value of such a waveform is given by

RMS value of primary current $= 10.7 \times \sqrt{0.5} = 10.7 \times 0.707 = 7.56$ A

7. Secondary current is a DC given by V_o/R_L.

Secondary current $= 1000/10000 = 0.1$ A

8. Primary and secondary wire sizes can be chosen for 7.56 A and 0.1 A, respectively.

15.5 Switching Regulators

Commonly used switching regulator configurations include *step-down* or *buck regulator*, *step-up* or *boost regulator* and *inverting regulator* also called *buck-boost regulator*. Each one of these configurations is briefly described in the following sections.

Buck Regulator

Figure 15.21 shows the basic buck regulator. It resembles the conventional forward converter discussed in Section 15.3 except for the fact that it does not use a transformer and there is no input–output isolation. Output voltage is always less than the input voltage and is given by $V_o = DV_{in}$, where D is the duty cycle ($= t_{ON}/T$) of the drive waveform to the transistor switch. Regulation is achieved by PWM of the drive waveform to the transistor switch. It is a very popular circuit configuration for fabrication of high-efficiency three-terminal switching regulators. The circuit operates as follows.

Transistor Q_1 acts like a single-pole, single-throw switch. When the transistor is turned ON, the voltage appearing at the emitter terminal of the transistor equals the input DC voltage assuming a zero drop across the collector–emitter terminals of the transistor. The current through the inductance L_1 ramps up to a value depending upon the input DC voltage, value of inductance and the turn-ON time. Diode D_1 during this time is reverse-biased. When the transistor is switched OFF, the polarity of voltage induced across the inductance reverses thus forward-biasing the diode D_1 called the free-wheeling diode. The diode clamps the voltage at emitter terminal of the transistor Q_1 to zero. Current through the inductance ramps down through the forward-biased free-wheeling diode during the time the transistor is switched OFF. Thus the voltage appearing across the input of LC filter is a waveform chopped between zero and the input DC voltage. The average value of this waveform is equal to $(V_{in} \times t_{ON}/T)$. The LC filter transforms this chopped waveform into a ripple-free DC output voltage.

A sample of the output voltage is compared with a reference voltage in an error amplifier. The output of the error amplifier is fed to a pulse width modulator circuit. The pulse width modulator is typically a comparator circuit whose other input is fed with a sawtooth waveform of appropriate amplitude. The output of pulse width modulator circuit feeds the switching transistor. The phasing of the feedback circuit comprising error amplifier and pulse width modulator circuit is such that an increase or decrease in output voltage by a

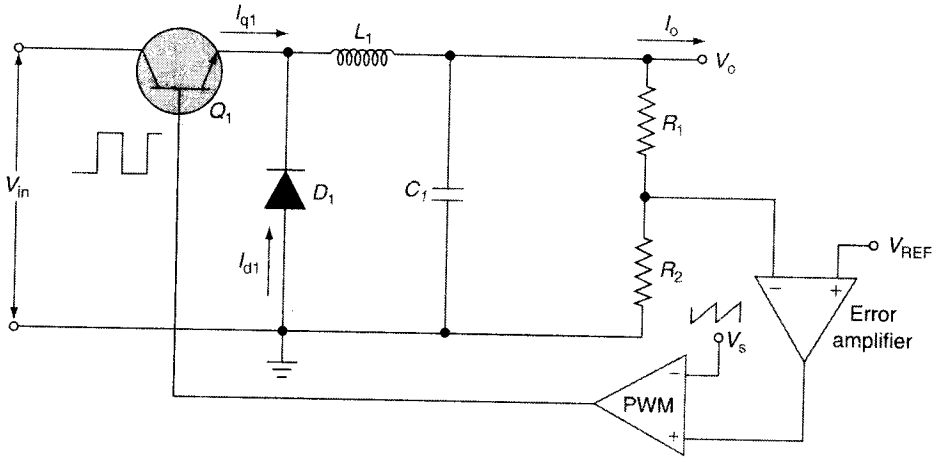


Figure 15.21 | Buck regulator.

certain percentage is accompanied by decrease or increase, respectively, in the ON-time of the switching transistor by the same percentage. The ON-time of the switching transistor Q_1 is so controlled as to make the sampled output voltage equal to the reference voltage applied to the error amplifier.

Figure 15.22 shows the relevant waveforms. These include the drive waveform to the base of transistor Q_1 [Figure 15.22(a)], voltage waveform appearing at the emitter terminal of the transistor Q_1 [Figure 15.22(b)], current waveform through the emitter terminal of Q_1 [Figure 15.22(c)], current waveform through free-wheeling diode D_1 [Figure 15.22(d)] and the output current I_o [Figure 15.22(e)]. The waveforms are self-explanatory.

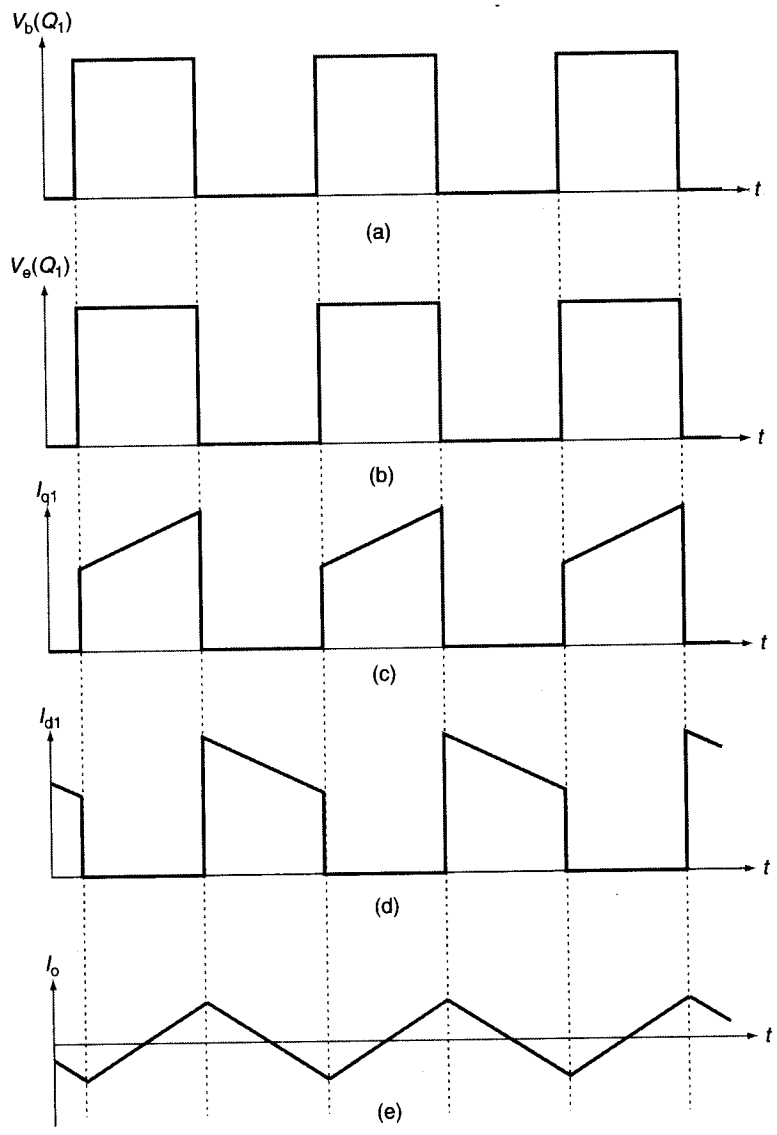


Figure 15.22 | Relevant waveform for buck regulator of Figure 15.21.

Boost Regulator

The step-up switching regulator, also called the *boost regulator* (Figure 15.23), is based on the flyback principle. It resembles the basic flyback converter except that it is non-isolating type. The energy storage and transfer element in this case is an inductor rather than a transformer. When the switching transistor Q_1 conducts, the inductor stores energy in the form of magnetic field. Energy stored equals $(1/2) \times (L_1 I_P^2)$. As the diode D_1 is reverse-biased during conduction time of the switching transistor, the energy cannot be transferred to the output while it is being stored. When the switching transistor is driven to cut-off, diode D_1 gets forward-biased and the stored energy is delivered to the load along with the energy from DC input voltage. The voltage across the load equals the DC input voltage plus the voltage due to the energy stored in the inductor. The output voltage in this case is given by $V_o = V_{in}/(1 - D) = V_{in} \times (T/t_{OFF})$. Here D is the duty cycle and T is the total time period which is equal to $t_{ON} + t_{OFF}$.

The power output capability of this circuit is equal to the sum of the power stored in the inductor and the power delivered to the load during the turn-OFF time. The former component is given by $(1/2) \times (L_1 I_P^2 f)$, where f is the operating frequency. The second component results from the fact that the decaying current ramp through the inductance during turn-OFF time is flowing through the source of DC. This equals $V_{in} \times (I_P/2) \times (t_{OFF}/T)$ for a discontinuous mode of operation and decaying ramp time equal to t_{OFF}. The output power-delivery capability of the boost converter is therefore given by

$$P_o = \frac{1}{2} \times (L_1 \times I_P^2 \times f) + V_{in} \times \left(\frac{I_P}{2}\right) \times \left(\frac{t_{OFF}}{T}\right) \tag{15.24}$$

The feedback circuit is similar to the one described in the case of buck regulator. Again, a sample of the output voltage is compared with a reference voltage in an error amplifier, whose output feeds one of the inputs of a pulse width modulator circuit. The other input to the pulse width modulator circuit is a sawtooth waveform. The output of pulse width modulator circuit feeds the switching transistor. The phasing of the feedback circuit comprising the error amplifier and the pulse width modulator circuit is such that the pulse width of the drive waveform increases or decreases with decrease or increase in the output voltage to keep the output voltage as constant irrespective changes in input DC voltage and load current changes.

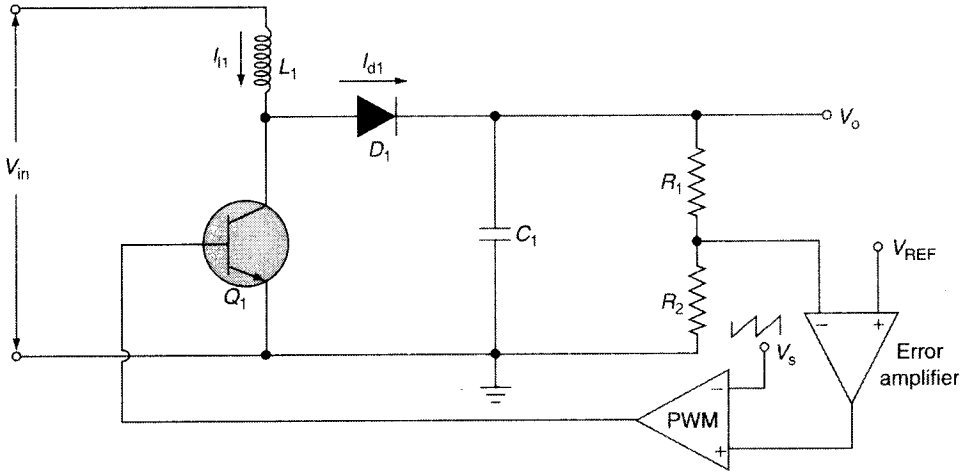


Figure 15.23 | Boost regulator.

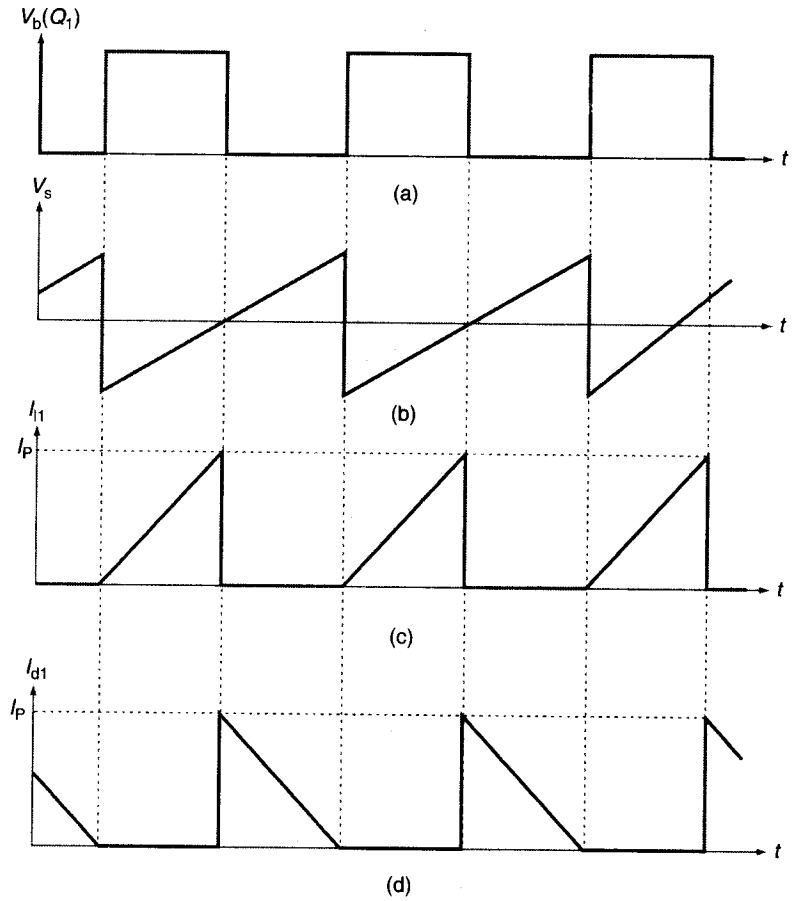


Figure 15.24 | Relevant waveforms for boost regulator of Figure 15.23.

Figure 15.24 shows the relevant waveforms. These include the drive waveform to the base of transistor Q_1, which is also the waveform at the output of pulse width modulator [Figure 15.24(a)], ramp voltage waveform appearing at one of the inputs to the pulse width modulator [Figure 15.24(b)], current waveform through the inductance L_1 [Figure 15.24(c)] and current waveform through diode D_1 [Figure 15.24(d)]. The waveforms are self-explanatory.

Inverting Regulator

Inverting regulator (Figure 15.25) is another circuit configuration based on the flyback converter principle. For a positive input, it produces a negative output. Energy is stored in the inductor (L_1) during the conduction time of the transistor. Diode D_1 is reverse-biased during this time period. The stored energy is transferred during the OFF-time. The circuit delivers a constant output power to the load. The output voltage is given by $-\sqrt{(P_o R_L)}$. Regulation of the output voltage, which is equal to $-V_{in} \times t_{ON}/t_{OFF}$ is achieved by controlling the duty cycle of the drive waveform. In the inverting regulator configuration, it is possible to have an output voltage that is either less than or greater than the input. It is also sometimes referred to as *buck-boost* regulator. Unlike the boost regulator, during the turn-OFF time period, the decaying current ramp

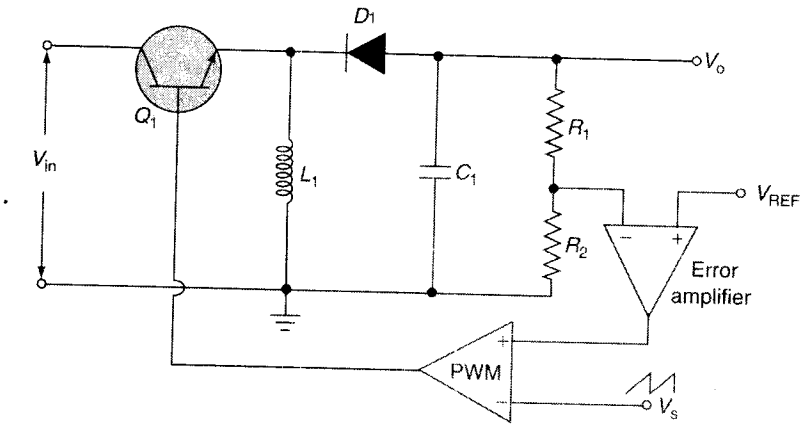


Figure 15.25 | Inverting regulator.

does not flow through the source of input DC. The output power-delivery capability of inverting regulator is therefore given by

$$P_o = \frac{1}{2} \times L_1 \times I_p^2 \times f \tag{15.25}$$

The waveforms are similar to those shown in the case of boost regulator.

Three-Terminal Switching Regulators

The basic buck regulator of Figure 15.21 has been widely exploited in the form of three-terminal switching regulators. Figure 15.26 shows the typical circuit configuration found inside such a regulator. Except for the switching transistor and the output inductor, all other component blocks have been integrated on the chip.

The output voltage is compared with a reference voltage and the difference is amplified to drive a pulse width modulator, which in turn operates the switch. The three-terminal regulator can be used to construct a step-down switching supply that works very well for a wide input voltage range (typically 4 to 1). Output power levels of 300 W are conveniently achievable.

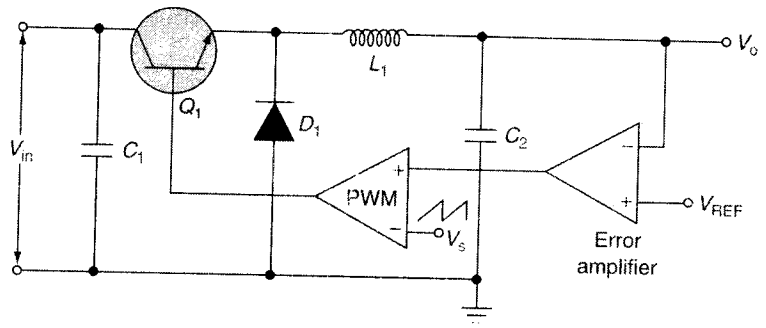


Figure 15.26 | Three-terminal switching regulator.

15.6 Connecting Power Converters in Series

Power converters can be connected in series in general but it is advisable to make checks with the specifications of the converters to be connected in series. It is possible that the output of one converter affects the feedback loop of the other. Another limitation on the series connection of the two converters is that the total output voltage of the series connected converters should not exceed the working breakdown voltage of any one of the power converters.

In order to protect each output from the reverse voltage of the other output in the event of a shorted-load condition, reverse-biased diodes should be connected across the output of each series-connected converter (Figure 15.27). Series connection can be used to get a higher output voltage. In a typical application, a dual-output power supply can be series connected to realize a single-ended supply with double output voltage (Figure 15.28).

15.7 Connecting Power Converters in Parallel

Power converters should be connected in parallel only when they have been specifically designed for the purpose or when the manufacturer recommends a parallel operation. The biggest problem in the parallel connection of the two converters arises from unequal load sharing. Unequal load sharing occurs primarily from the following reasons.

The output voltages of the converters are not precisely equal. The converter with greater output voltage will tend to provide the entire load current. Even if the output voltages are adjusted to be precisely equal, a difference in the output impedance and also its drift with time and temperature will cause the loads to become unbalanced.

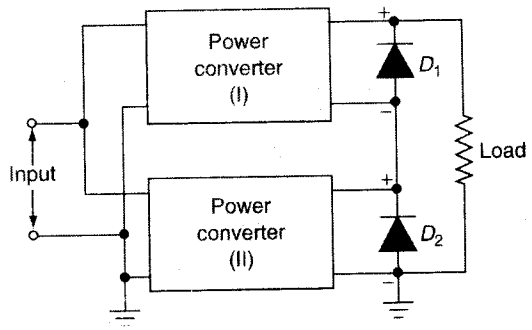


Figure 15.27 | Series connection of power converters.

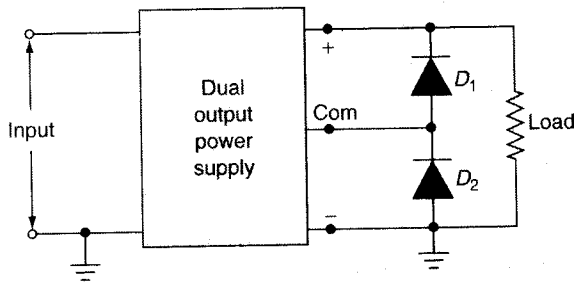


Figure 15.28 | Series connection of dual-output power supply.

One method used to overcome this unequal load sharing is to use small individual series resistors (Figure 15.29). While this type of parallel connection could be useful in a few applications, it must be borne in mind that the series resistors degrade the output regulation seriously. Also, the circuit will always have current imbalance. If the two converters in Figure 15.29 had a nominal output voltage of 5 V, a 50 mV difference in the output voltages may cause a current imbalance of 25%. In such a case, each supply should not be capable of providing just 50% of the load current but 75% of it.

A good reason for parallel connection of power converters is to provide redundancy. The output may be connected in parallel through two diodes (Figure 15.30). For 100% redundancy, each power converter must be capable of supplying the total load current. In this case, it really does not matter whether the load is shared equally or not, though it is desirable that each output provides at least a part of the load current. The diodes permit one output to fail without affecting the other, which continues to supply the power to the load. Such a system is useful in applications where power supply failure is not tolerable, or where a high degree of reliability is required. If one of the power converters is replaced by a DC battery source of the same voltage, it becomes an uninterrupted DC power supply (Figure 15.31).

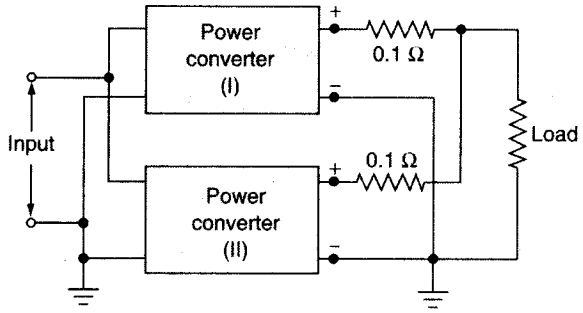


Figure 15.29 | Parallel connection of converters using series resistors.

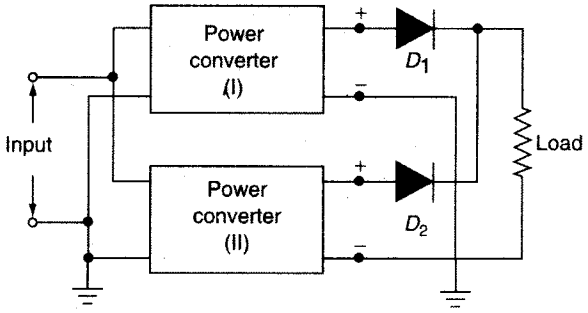


Figure 15.30 | Parallel connection of converters using diodes.

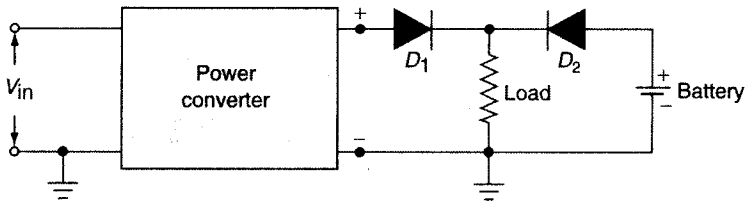


Figure 15.31 | Uninterrupted power supply.

EXAMPLE 15.4

Figure 15.32 shows the basic buck regulator configuration. It produces a regulated output voltage of +12 V. If the unregulated input voltage at a certain time is +24 V, determine the ON-time of the drive waveform appearing at the base terminal of the switching transistor Q_1. Assume a switching frequency of 10 kHz.

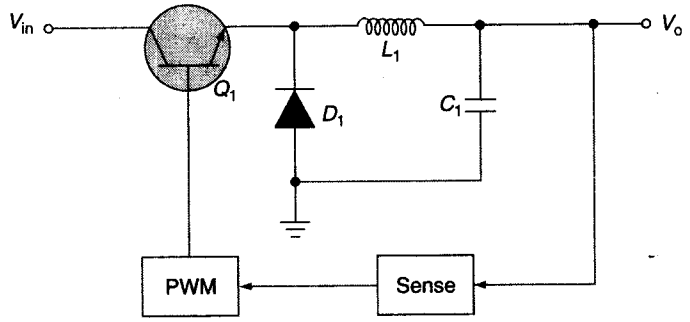


Figure 15.32 | Example 15.4.

Solution

The output voltage in the case of buck regulator is given by

$$V_o = V_{in} \times (t_{ON}/T) = V_{in} \times t_{ON} \times f$$

$$t_{ON} = V_o/(V_{in} \times f) = 12/(24 \times 10^4) = 50\ \mu s$$

EXAMPLE 15.5

Figure 15.33 shows the basic boost regulator circuit using a pulse width modulated drive waveform control (V_{in} = 12 V). For the drive waveform shown in the circuit, determine the output voltage. Also, determine the changed ON-time of the drive waveform when the unregulated input voltage changes to +18 V.

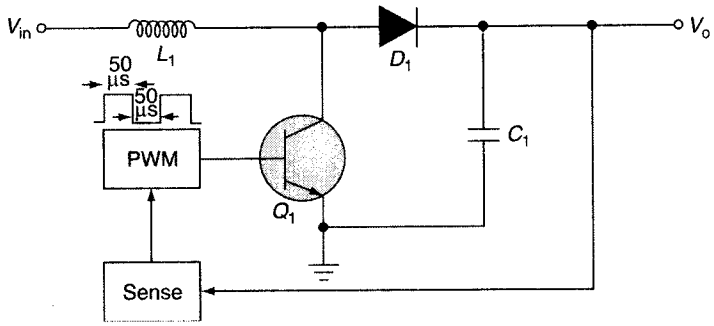


Figure 15.33 | Example 15.5.

Solution

1. From the given drive waveform, duty cycle, $D = (50 \times 10^{-6})/(50 \times 10^{-6} + 50 \times 10^{-6}) = 0.5$.
2. The output voltage V_O in the case of boost regulator configuration is given by $V_o = V_{in}/(1 - D) = 12/(1 - 0.5) = 24$ V.
3. When the input voltage changes to + 18 V, the new value of duty cycle D required to maintain the output voltage at + 24 V is given by

$$24 = 18/(1 - D)$$
$$D = 1 - (18/24) = 0.25$$

4. Therefore, the changed value of on-time is given by $0.25 \times 100 \times 10^{-6} = 25$ μs.

EXAMPLE 15.6

Figure 15.34 shows the basic inverting regulator circuit using a pulse width modulated drive control. Determine the output voltage if the switching frequency were 10 kHz.

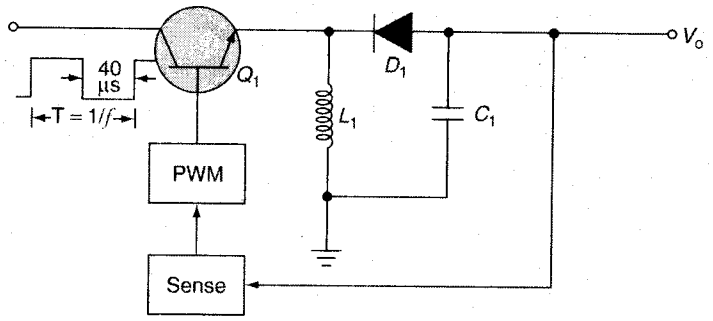


Figure 15.34 Example 15.6.

Solution

1. The output voltage is given by $V_o = -V_{in} \times (t_{ON}/t_{OFF})$.
2. From the given drive waveform, t_{OFF} = 40 μs, f = 10 kHz. This gives $T = 1/10^4$ s = 100 μs.
3. Therefore, $t_{ON} = 100 - 40 = 60$ μs.
4. This gives $V_o = -18 \times (60/40) = -27$ V.

KEY TERMS

Boost regulator
Buck-boost regulator
Buck regulator
Continuous mode
Discontinuous mode
Flyback converter
Forward converter
Full-bridge converter
Half-bridge converter
Inverting regulator
Push–pull converter
Switched mode power supplies

OBJECTIVE-TYPE EXERCISES

Multiple-Choice Questions

1. In a flyback DC-to-DC converter, the energy is stored in the primary winding of the switching transformer during
   a. turn-ON time of the switching device.
   b. turn-OFF time of the switching device.
   c. both turn-ON and turn-OFF times of the switching device.
   d. none of these.

2. Which of the following statements is true in the case of ringing-choke power converter during turn-ON time of the switching transistor?
   a. Energy stored, fast recovery rectifier forward-biased, filter capacitor charging
   b. Energy transferred, fast recovery rectifier reverse-biased, filter capacitor charging
   c. Energy stored, fast recovery rectifier reverse-biased, filter capacitor discharging
   d. Energy transferred, fast recovery rectifier forward-biased, filter capacitor charging

3. Which of the following expressions can be used to determine the output voltage in the case of self-oscillating flyback DC-to-DC converter?
   a. $V_o = \sqrt{P_o \times R_L}$
   b. $V_o = n \times V_{in}$ (n is the step-up ratio of the switching transformer)
   c. $V_o = \eta \times V_{in}$ (η is the conversion efficiency)
   d. $V_o = \sqrt{P_o / R_L}$

4. A DC-to-DC converter having a conversion efficiency of 80% is delivering a power of 16 W to the load. If the converter were producing an output voltage of 400 V from an input of 20 V, what would be the current drawn from the 20 V source?
   a. 1000 mA
   b. 500 mA
   c. 200 mA
   d. Cannot be determined from given data

5. Figure 15.35 shows the secondary current waveform in the case of
   a. forward-type DC-to-DC converter.
   b. flyback-type DC-to-DC converter.
   c. Buck-type switching regulator.
   d. none of these.

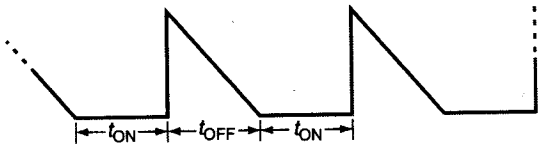


Figure 15.35 | Multiple-choice question 5.

6. The effect of core saturation on primary inductance is
   a. constancy of primary inductance.
   b. sudden increase in primary inductance.
   c. sudden decrease in primary inductance.
   d. core saturation has no effect on primary inductance.

7. Cutting an air gap in the magnetic path of a core
   a. produces a relatively lower B for a given H.
   b. produces a relatively higher B for a given H.
   c. increases the core permeability.
   d. none of these.

8. Which component size is affected by frequency of operation of converter?
   a. Transformer and transistor
   b. Transformer and filter capacitor
   c. Switching transistor and filter capacitor
   d. Switching transistor, transformer, filter capacitor

9. The maximum value of primary current that can flow in a push–pull converter when either of the transistors is conducting is given by one of the following expressions.
   a. $(P_o/\eta V_{in}) + (V_{in}/4fL_p)$
   b. $P_o/\eta V_{in}$
   c. $V_{in}/4fL_p$
   d. None of these

10. An air gap of length equal to one-hundredth of the magnetic path length of a ferrite core with initial permeability of 3000 will reduce permeability to
    a. approximately 100.
    b. approximately 300.
    c. approximately 30.
    d. none of these.

Identify the Switching Regulator Configurations

Identify the switching regulator circuits shown in Figures 15.36(a)–(f). Choose from buck regulator, boost regulator, inverting regulator, flyback DC-to-DC converter, forward DC-to-DC converter and push–pull DC-to-DC converter.

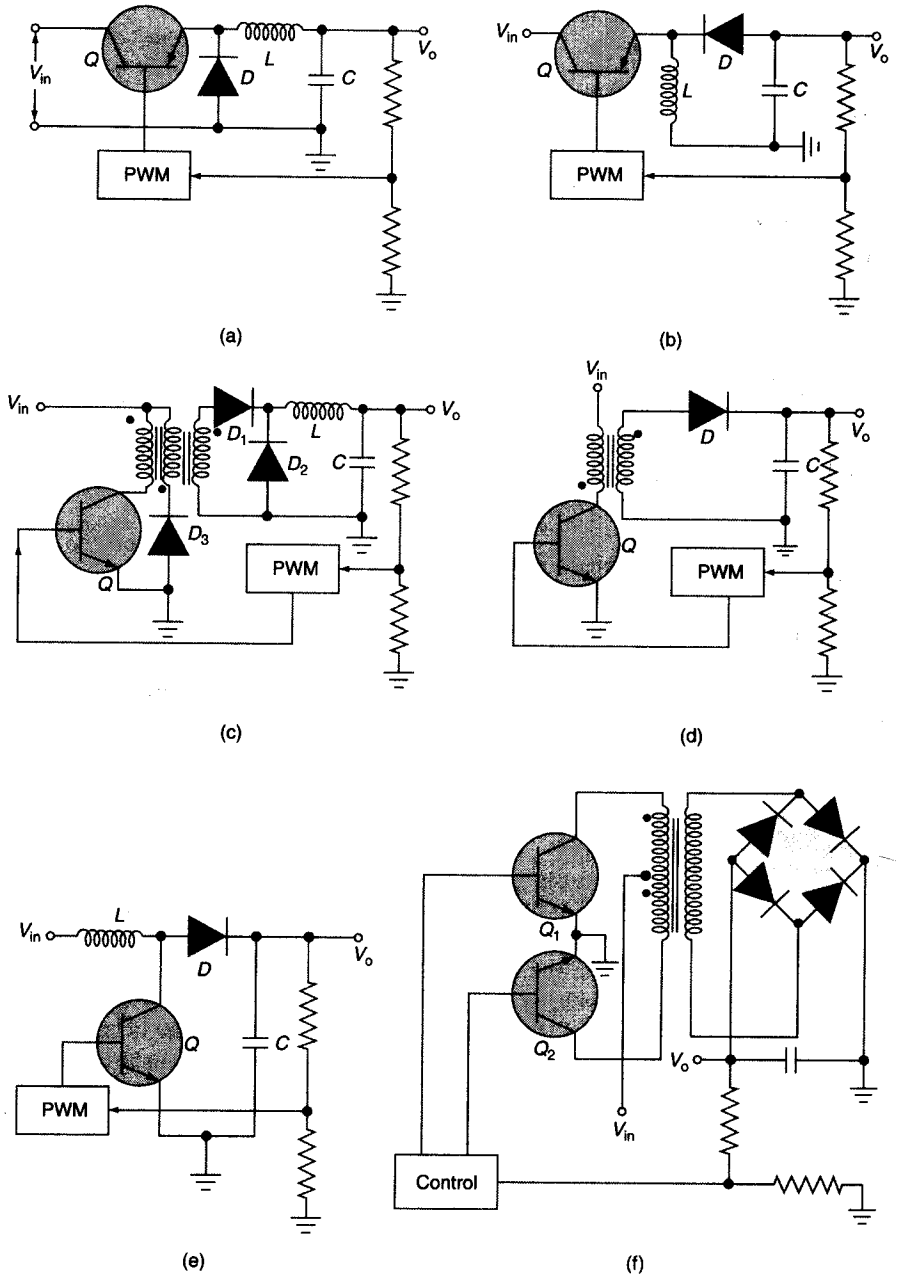


Figure 15.36 | Identify the switching regulator configurations.

REVIEW QUESTIONS

1. Distinguish between a linearly regulated power supply and a switched mode power supply with particular reference to their principle of operation, advantages and disadvantages.
2. With the help of circuit schematic and relevant waveforms, briefly describe the principle of operation of a self-oscillating or ringing-choke DC-to-DC converter. Explain why such a converter is termed as a constant output power converter?
3. Briefly describe the procedure for designing a flyback DC-to-DC converter operating from an input voltage of V_{in} and required to deliver an output power of P_o to the load.
4. Give reasons for the following:
   a. Why is a flyback DC-to-DC converter not suitable for delivering high levels of power to the load?
   b. Why is peak primary current relatively much higher in the case of flyback DC-to-DC converter operating in discontinuous mode as compared to the one operating in continuous mode for the same output power-delivery capability?
   c. Why can the boost regulator configuration not produce an output voltage less than the input voltage?
   d. Why does parallel connection of power converters to get higher load current delivery capability put very stringent output impedance requirement on the individual converters?
5. Briefly describe the operational principle of push–pull DC-to-DC converter. What are the advantages of using half-bridge and full-bridge configurations over the conventional push–pull configuration?
6. With the help of basic circuit configurations, briefly describe the operational principle of the following switching regulator circuits:
   a. Buck regulator
   b. Boost regulator
   c. Buck-boost regulator
7. Which regulator configuration is used in three-terminal switching regulators?
8. Why do we need to connect power converters in series or parallel? What are the special measures that we need to take while doing so?

PROBLEMS

1. A ringing-choke-type DC-to-DC converter is designed to deliver 100 W of power to a load resistance of 10 kΩ. Determine the output voltage. How would the output voltage change if the load resistance changes to 8.1 kΩ?
2. The switching transformer for a flyback-type DC-to-DC converter has to sustain a volt-second product of 6×10^{-4} V s and a maximum flux density of 2000 Gauss. Determine the minimum cross-sectional area of the core required to achieve this if the number of primary turns used to get the desired inductance were 50.
3. A step-down switching regulator of the type shown in Figure 15.21 is used to produce a regulated output of 12 V from an unregulated input of 18–24 V. If the switching transistor were switched at 20 kHz, determine the turn-ON time of the switching transistor for unregulated input voltages of 18 V and 24 V.
4. Refer to the basic boost regulator configuration of Figure 15.23. The switching regulator operating at a switching frequency of 10 kHz is fed with an unregulated input voltage of 9–15 V and produces a regulated output voltage of 24 V.

a. Determine the turn-ON time of the drive waveform at the time instant when the input voltage was measured to be 12 V.

b. Determine the input voltage at the time instant when the duty cycle of the drive waveform was measured to be 0.6.

5. Refer to the inverting regulator circuit of Figure 15.25. The regulator is switched at 20 kHz. The regulator produces a regulated output voltage of −12 V from an unregulated input of 9–15 V. Determine the turn-ON and turn-OFF times of the drive waveform for input voltages of (a) 9 V and (b) 15 V.

ANSWERS

Multiple-Choice Questions

1. (a)	**3.** (a)	**5.** (b)	**7.** (a)	**9.** (a)
2. (c)	**4.** (a)	**6.** (c)	**8.** (b)	**10.** (a)

Identify the Switching Regulator Configurations

Figure 15.36(a): Buck regulator
Figure 15.36(b): Inverting regulator
Figure 15.36(c): Forward converters
Figure 15.36(d): Flyback converter
Figure 15.36(e): Boost regulator
Figure 15.36(f): Push–pull converter

Problems

1. 1000 V, 900 V

2. 0.6 cm^2

3. 33.33 μs, 25 μs

4. (a) 50 μs; (b) 9.6 V

5. (a) $t_{ON} = 28.6$ μs, $t_{OFF} = 21.4$ μs;
(b) $t_{ON} = 22.2$ μs, $t_{OFF} = 27.8$ μs